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PROCESSING OPTIONS FOR EMBEDDED-SYSTEM DESIGNS

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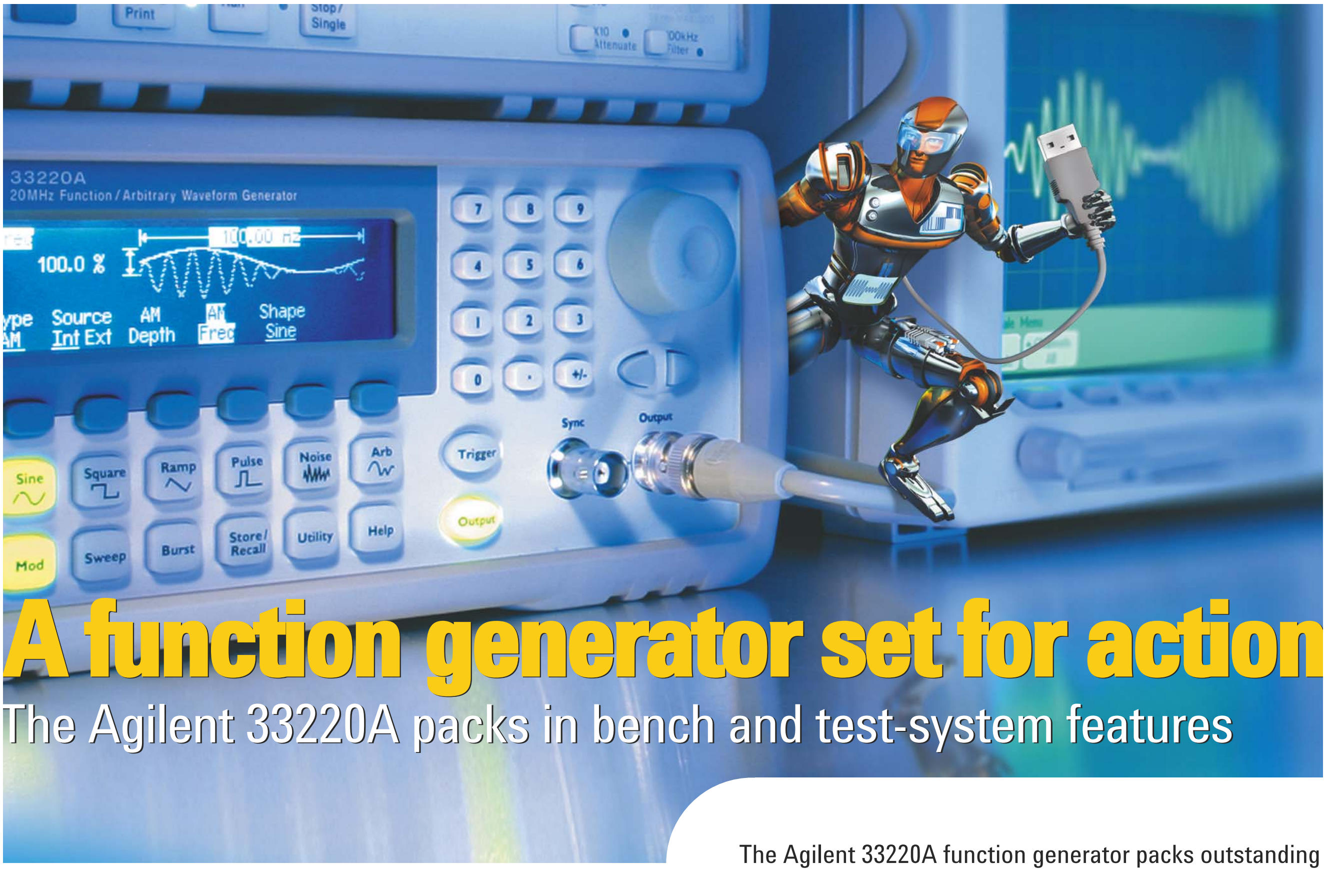

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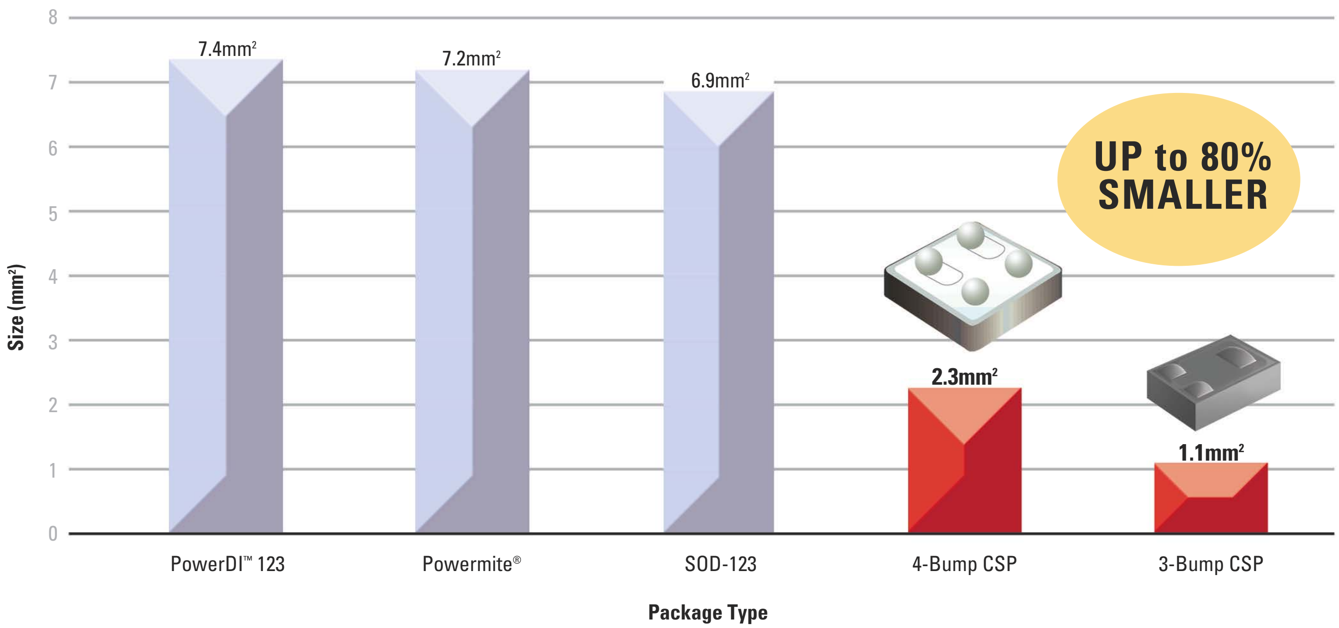

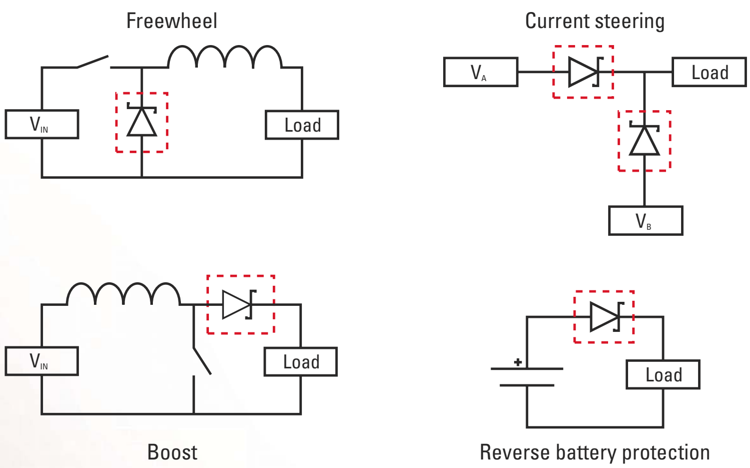

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IR05H40CSPTR	0.5A	40V	0.42V	10µA	-55 to 150°C
IR130CSPTR	1.0A	30V	0.33V	100µA	-55 to 150°C
IR140CSPTR	1.0A	40V	0.38V	80µA	-55 to 150°C
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ANALOG DEVICES

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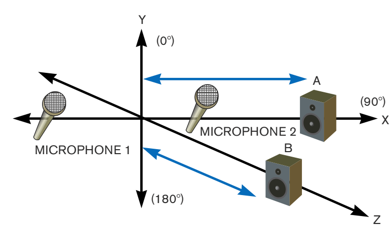
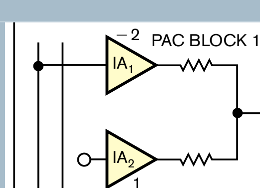


DESIGNIDEAS



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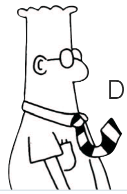

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DEPARTMENTS & COLUMNS

PRODUCT ROUNDUP

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A New Approach to Streamlining the Application of Advanced Technologies

Today's increasing silicon complexity drives engineers to continually leverage the latest advances in electronic design. However, no company can afford to have its design teams consuming time and effort adopting individual technologies. Instead, organizations need to focus precious engineering resources where they add the most value—differentiating the company's designs. Additionally, in today's fast-paced markets, missed schedules can mean lost market opportunities. Cadence recognizes that to start designing right away, designers need a proven infrastructure—proven on the types of designs they'll be doing and incorporating the kind of IP they'll be incorporating—with typical application hurdles already flattened. This is the essence of the Cadence Kits approach.

A Cadence Kit is a documented methodology built on a set of platform flows applied to a reference design, which is enabled by standards-based IP and packaged with applicability training. Each kit starts with a reference design—a real design representing a specific vertical market.

The reference design incorporates IP that is integrated and validated with the platform flows. One of the biggest challenges has been the difficulty of using IP in the design process. By building on platform flows and a reference design, Cadence Kits greatly simplify the integration, reuse and enablement of IP.

DELIVERING ON THE KITS APPROACH

The first Cadence Kit focuses on analog/mixed-signal (AMS) because of its pervasiveness across markets, including wireless, wired networking, and personal entertainment electronics. The AMS Methodology Kit minimizes risk by targeting key challenges identified by customers in these markets:

- Fragmented design processes that prevent teams from effectively verifying designs across the analog and digital design domains
- Large quantities of data and long simulations, which hamper modeling, extraction and re-simulation of parasitics
- The challenge of managing multiple power supplies through all stages of design as well as reusing and migrating AMS blocks—both of which demand a predictable methodology

The Cadence AMS Methodology Kit addresses these design challenges by delivering a verified methodology, enabling IP, and applicability training—all demonstrated on an end-to-end mixed-signal design.

The AMS Methodology Kit executes a "meet in the middle" design approach that achieves an optimum balance between the needs for speed and for silicon accuracy. It also establishes a design process that allows teams to work with the analog/mixed-signal content in the context of the complete design—from concept to silicon.

The kit gives designers control of parasitic effects from first-cut route and top-level parasitic extraction evolving to block-level and targeted post-layout re-simulation. It addresses reuse and migration of analog/mixed-signal blocks through a repeatable block creation method. In addition, the AMS Methodology Kit helps teams tackle low-power designs by managing multiple power supplies through a top-down methodology for defining voltage supplies.

For more information on how Cadence Kits enable you to simplify the application of EDA technology for greater design productivity, visit www.cadence.com/kit_info.

EDN online contents

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THE TOP 10 ARTICLES OF 2005

Based on traffic to www.edn.com. For the complete top 30, see www.edn.com/article/CA6294184

Circuit makes simple high-voltage inverter
→www.edn.com/article/CA419572

2005 Microprocessor Directory: Charting your course
→www.edn.com/microdirectory

The Hot 100 products of 2004
→www.edn.com/article/CA486570

Circuit provides bidirectional, variable-speed motor control
→www.edn.com/article/CA216168

Using the HID class eases the job of writing USB device drivers
→www.edn.com/article/CA243218

Build a transformerless 12V-to-180V dc/dc converter
→www.edn.com/article/CA431146

Circuit generates fan-speed control
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HDCP: what it is and how to use it
→www.edn.com/article/CA209091

Black boxes capture car-crash data, controversy
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Filters in a nutshell: Spreadsheet promotes intuitive feel
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ONLINE ONLY

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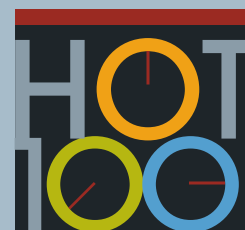
Magma takes spotlight in Synopsys survey

Synopsys, Cadence, and Mentor may be giving up customers to Magma in the next physical-design-tool buying cycle, but users are generally pleased with Synopsys in comparison with its archrival Cadence, according to the latest survey published by EDA-industry gadfly John Cooley.
→www.edn.com/article/CA6293801

SiGe power amp targets PHS handsets to WiFi

Toshiba based its new TA4401CT power amplifier on three cascaded RF stages that target linearity, efficiency, and low power in wireless applications in bands ranging from 1.9 to 2.5 GHz.
→www.edn.com/article/CA6293328



AUDIOCAST: *EDN*'s HOT 100 PRODUCTS OF 2005

In case you missed it, *EDN* published its annual list of the 100 most significant products of the past year in the December 16, 2005, issue. Check out the URL below to review the products that made the cut. While you're there, click on the "audiocast" link to hear Editor in Chief Maury Wright comment on some of the key products and the trends they represent.
→www.edn.com/article/CA6290449

FROM THE VAULT

Articles and extras from the EDN *archives that relate to this issue's contents.*

PROCESSING OPTIONS (pg 42):

Control and signal processing: Can one processor do it all?
→www.edn.com/article/CA198914

EDN hands-on project:
Part 1: Accelerate your performance
→www.edn.com/article/CA476908

Part 2: Automate your acceleration
→www.edn.com/article/CA484490

Operating alone
→www.edn.com/article/CA6288032

VARIATIONS ON A THEME (pg 53):

Got game? Living-room consoles grapple for eyes, wallets
→www.edn.com/article/CA6290451

Gaming as serious business
→www.edn.com/article/CA193186

Prying Eyes: In the game?
→www.edn.com/article/CA605509

ACCURATELY JUDGING ENDURANCE FOR SOLID-STATE STORAGE (pg 67):

Pick a card: card formats
→www.edn.com/article/CA431145

CLEAR CALLS FROM THE ROAD (pg 71):

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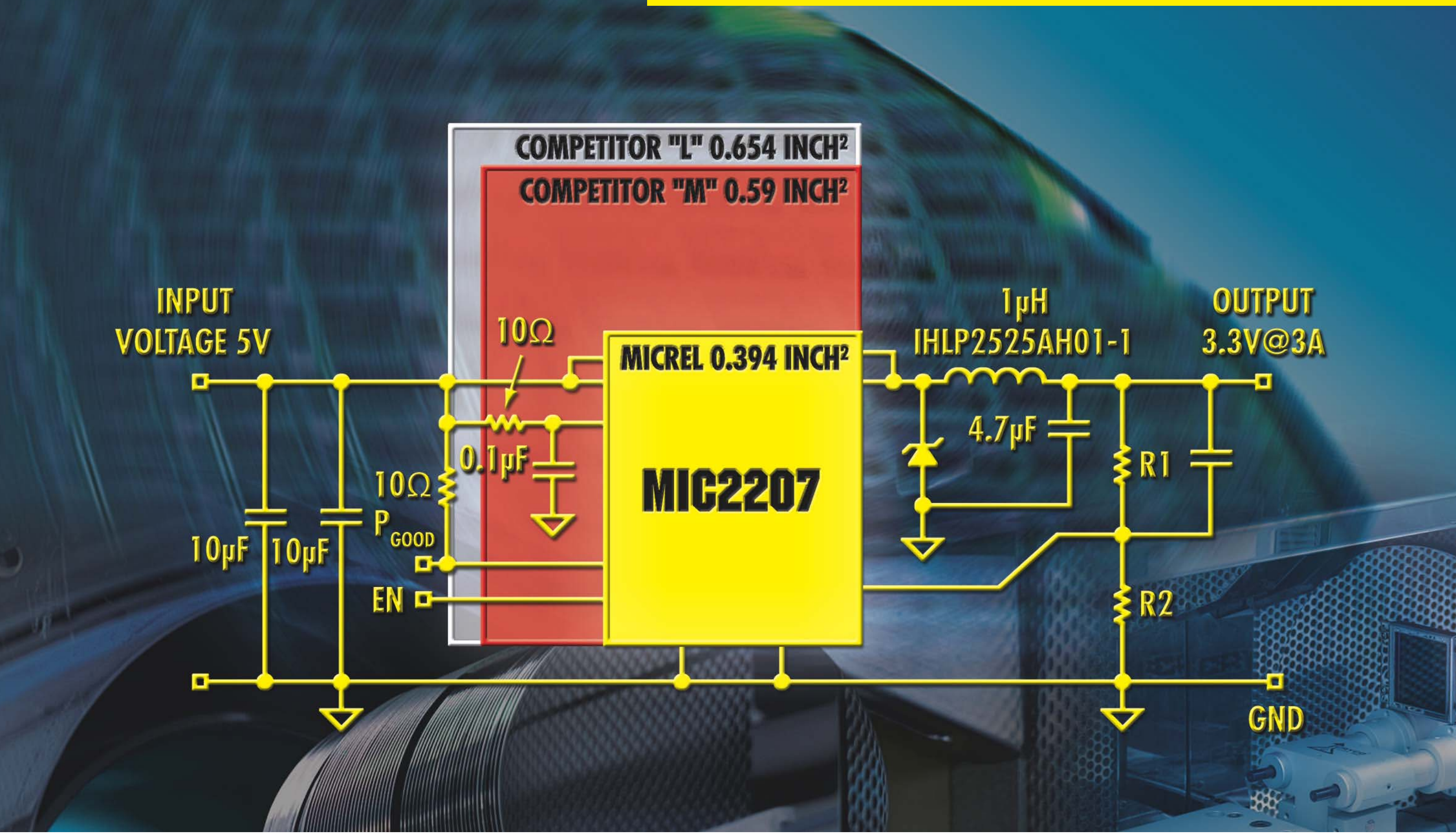

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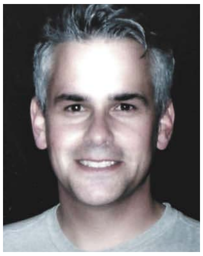

BY MICHAEL SANTARINI, SENIOR EDITOR

EDA industry needs a reality check

Four years ago, the EDA industry appeared to be on top of the world; now, it appears to be taking desperate measures to show a recovery. In 2001, when every other industry was struggling under the weight of the worst recession in modern times, the big three EDA vendors were putting up solid but not stellar revenue gains, and EDA start-ups accounted for three of the top 10 IPOs (initial public offerings) across all industries.

EDA's seemingly brightest moment in what turned out to be a supernova of a year came at an EDAC (EDA Consortium) Chief Executive Officer forecast panel. EDAC organizers were beaming because, after a seemingly eternal absence, reporters from the business press had shown up at an EDA event. A bunch of smiling new faces, mostly bankers and venture capitalists, gathered to hear the prospects of what appeared to be a bulletproof industry. It was a standing-room-only event. The place was buzzing.

During that panel, the chief executive officers stayed away from the esoteric engineering stuff they usually offer us in the trade press and instead gave a simple, unified message: EDA is recession-proof. They espoused the view that their customers, though struggling and madly laying off employees, still needed to innovate to get out of the downturn and therefore wouldn't cut R&D budgets. EDA-industry chiefs also touted the fact that the industry would ease the lives of analysts, investors, and maybe even customers by doing away with perpetual licensing. Instead, it would offer customers one- to three-year subscriptions. Doing so, they said, would relieve their sales forces of cutting deals in the 11th hour of each quarter to meet quotas.

That moment was a high point for the EDA industry, but it didn't take long for reality to kick in. About six months later, the EDA industry learned the long, hard lesson that it is not recession-proof but rather a recession indicator. Since then, the EDA industry has been desperately trying to show that it is an indicator of a recovery. It hasn't yet recovered, but, sadly, it appears to be desperate to show that it has. Indeed, several reports from the field claim that EDA vendors are avidly discounting tools and even offering all-you-can-eat-buffet licensing to their biggest customers, further delaying the industry's recovery.

If the EDA industry wants to turn the tide, it should stop dealing out marketing bull and address the weak points.

But perhaps the biggest sign of desperation occurred too quietly in October 2005, when the EDAC's MSS (Market Statistics Service) quietly issued second-quarter earnings claiming that industry revenue was flat (**Reference 1**). For the first time, EDAC didn't offer a spokesman to comment on the quarter. That exception should have been the first indicator that something was fishy with MSS' account of the quarter. A closer look at the release shows that true EDA, which comprises tools, maintenance, and services (in a good year), is in fact *down*; roughly 20% of $1.09 billion in EDA revenue for the quarter came from IP (intellectual-property) revenue, not traditional EDA.

It is as if EDAC had simply decided that, if traditional EDA isn't going to recover soon, it will just expand the definition of EDA. The worst part isn't that EDAC MSS is reporting the revenue traditional EDA companies also gain in their side IP businesses; it's that the organization now counts revenue from pure-play IP companies, such as MIPS Technologies, as EDA.

It's sad that EDAC has had to stoop so low as to so overtly manipulate the numbers. It is even worse that the industry press, which actively reports industry earnings, regurgitated the press release and didn't question MSS' numbers. If the EDA industry wants to turn the tide, it should stop dealing out marketing bull, take a realistic look at the state of its business, and address the weak points. The online version of this column at www.edn.com/060119ed lists seven issues that the EDA industry needs to address. I'd be happy to hear your suggestions, too, for what I deem an essential but painfully misrepresented industry. E-mail me at michael.santarini@reedbusiness.com. EDN

REFERENCE

1 www.edac.org/downloads/pressreleases/05-10-05_MSS_Q2_2005_Release.pdf.

ANALOG | edge[SM]

Expert tips, tricks, and techniques for analog designs

Vol. IV, Issue 1

DESIGN | idea

High-Performance Analog Front Ends

by Ian King, Senior System Engineer

High-Speed Signals

High-speed conversion systems, especially in the telecommunications field, allow the input to the ADC to be AC-coupled either through a transformer, a capacitor, or a combination of both. For the test and measurement industry however, the front-end design is not as simple because this application area often requires the input signal to be DC-coupled as well as provide the capability for AC-coupling. The design of an active front end that delivers good pulse response and low distortion from DC up to frequencies of 500 MHz (and beyond) is challenging. This issue of the Analog Edge[SM] will provide a few design ideas and suggestions for an analog front end for use with high-performance ADCs suitable for high-speed data capture.

The preferred method of interfacing high-frequency analog signals to the input of an ADC is through the use of differential amplifiers. Therefore, the first component to be selected should be a differential output operational amplifier. When choosing such a device, there are two main considerations: the gain bandwidth product and the ability to set the common-mode output voltage of the op amp from an external voltage. This is because it is very important that the signal amplifier driving the ADC's inputs has its common mode output voltage (V_{CMO}) set within the optimum range for the ADC. If this condition is not met, the ADC's performance will rapidly degrade as the disparity between the amplifier's V_{CMO} and the ADC's optimum input common mode voltage increase.

The main disadvantage of wideband differential op amps is that they usually have limited gain and may also have their gain level preset internally. Depending on the application, it may be necessary to add a pre-amplifier to the design to meet the necessary gain requirement.

For the pre-amplifier, a very wideband op amp should be used in order to meet the desired input frequency of the ADC. For systems which sample up to 1 GSPS, this equates to an input bandwidth requirement of 500 MHz for over sampling systems.

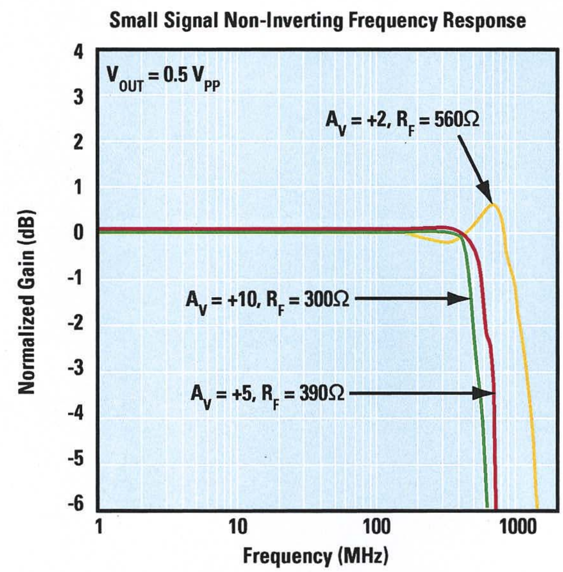

Figure 1. LMH6703 Frequency Response

For an operational amplifier to operate with significant gain (A_V=10 for example) and maintain such a wide bandwidth, equates to a 5 GHz Gain Bandwidth (GBW) product. Most voltage feedback amplifiers will not be able to meet this specification due to the direct tradeoff between frequency response and gain inherent in this architecture. Current feedback amplifiers however, enjoy a much better relationship between these parameters because the performance is generally dictated by the value of the feedback resistor within the op-amp circuit. An op amp that is ideal for operating at high bandwidths with gain settings between 1 and 10 is the LMH6703. This device can be used with the selected differential amplifier to provide any extra gain requirements in high bandwidth systems such as oscilloscopes and data capture cards.

The frequency response of this particular amplifier can be seen in *Figure 1*.

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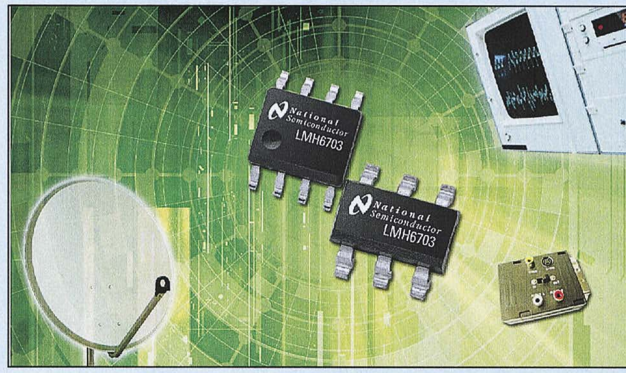
The unique folding and interpolating architecture, fully differential comparator design, innovative design of the internal sample-and hold amplifier, and the self-calibration scheme enable a very flat response of all dynamic parameters beyond Nyquist.

Features

- 7.25 Effective number of bits (ENOB) at Nyquist, 1.5 GSPS (typ.)
- Bit error rate 10^{-18} (typ.)
- Interleave mode on the ADC08D1500 for up to 3 GSPS sampling
- Choice of SDR or DDR output clocking
- Multiple ADC synchronization capability
- Serial interface for extended control
- Fine adjustment of input full-scale range and offset
- Single +1.9V (±0.1V) operation
- ADC08D1500 Consumes only 1.8W while running at 3 GSPS
- ADC081500 Consumes only 1.2W while running at 1.5 GSPS

The ADC08D1500 and the ADC081500 are well suited for a variety of applications including direct RF down conversion, digital oscilloscopes, satellite set-top boxes, communications systems, and test instrumentation. These converters are available in LQFP-128 packaging.

www.national.com/pf/DC/ADC081500.html
www.national.com/pf/DC/ADC08D1500.html



1.2 GHz, Low Distortion Op Amp with Shutdown

The LMH6703 is a very wideband, DC coupled monolithic operational amplifier designed specifically for ultra-high resolution video systems as well as wide dynamic range systems requiring exceptional signal fidelity. Benefiting from National's current feedback architecture, the LMH6703 offers a practical gain range of ±1 to ±10 while providing stable operation without external compensation, even at unity gain. At a gain of +2, the LMH6703 supports ultra high resolution video systems with a 750 MHz 2 V_{PP} -3 dB bandwidth.

With 12-bit distortion levels through 10 MHz ($R_L = 100\Omega$), and a 2.3 nV/$\sqrt{Hz}$ input referred noise, the LMH6703 is the ideal driver or buffer for high speed flash A/D and D/A converters. Wide dynamic range systems requiring exceptional signal fidelity and low distortion, such as in the test and measurement markets, can benefit from the performance of the LMH6703 amplifier.

Features

- -3 dB Bandwidth (V_{OUT} = 0.5 V_{PP}, A_V = +2) 1.2 GHz
- Fast slew rate 4500 V/µs
- 2nd/3rd Harmonic (20 MHz, SOT23-6) -69/-90 dBc
- Low noise 2.3 nV/$\sqrt{Hz}$
- Low differential gain and phase 0.01%/0.02°

The LMH6703 is ideal for use in video switching and distribution, radar, communication receivers, and test and measurement applications, and is available in SOIC-8 and SOT23-6 packaging.

www.national.com/pf/LM/LMH6703.html

High Performance Analog Front Ends

For a gain setting of 10 and a bandwidth of 500 MHz, the graph in ***Figure 1*** recommends the feedback resistor (RF1) to be 300 Ohms.

$$Av = 1 + (Rf / Rg)$$

Therefore RG1 (the gain resistor) can be selected as 33 Ohms.

As an example, ***Figure 2*** below shows the LMH6703 in circuit with a differential amplifier.

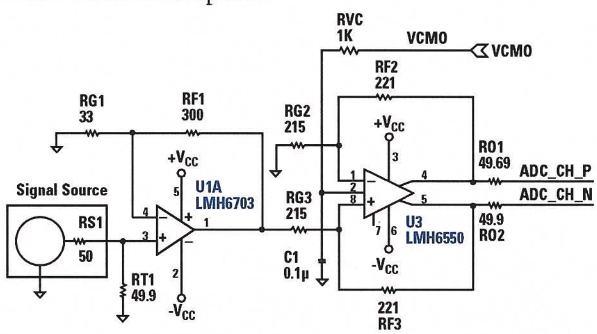


Figure 2. Two Stage Amplifier Circuit Diagram

Having provided the system with suitable levels of fixed gain for the DC signal path, the application may also require an AC-coupled mode. This is because a DC signal path will always be restricted by the gain bandwidth produced by the input amplifier. For data capture devices or communications channels that require very wide input bandwidth and low distortion, an AC signal path may be used. This allows the upper input frequency limit to extend beyond the DC signal path capability.

This can be solved in a number of ways and the choice of which method will depend largely on the minimum input frequency and the required high frequency performance. For ultimate AC performance at high frequencies (200 MHz and above), balun transformers offer a good solution to achieve single-ended-to-differential conversion as they add very little distortion to the signal. The trade off is that baluns are lossy components which will attenuate the signal by a small amount (-1 to 2 dB) and they also have poor low-frequency performance. A balun-coupled signal path can be inserted into the circuit of ***Figure 3*** by using a single-pole RF relay to switch the single-ended output signal from the pre-amplifier into either the differential amplifier or the Balun Circuit. A 2nd Double Pole Double Throw RF relay is also required to route the outputs of the balun and differential amplifier into the ADC inputs.

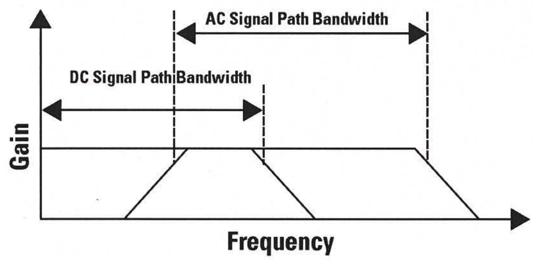


Figure 3. Frequency Response of a System with Extended AC Signal Capability

This circuit works well for high-end test and measurement equipment. But for cost-sensitive applications, the cost of RF signal relays becomes a burden on the system budget, especially if multiple channels are required. It is therefore advantageous for lower-speed systems to select a differential output operational amplifier that can be used for both AC- and DC-coupled modes, thus eliminating the balun circuit. Amplifiers suitable specifically for this task are beginning to gradually appear and are offering increasing performance in terms of bandwidth and THD figures. For an 8-bit 1 GSPS converter, a differential amplifier offering -50 dB THD figures at 500 MHz with a minimum bandwidth of 1 GHz, would be a good set of parameters to seek out. Good dynamic performance can be obtained from high-speed ADCs using off the shelf op-amp components in the front end design which greatly reduce the design time. The SINAD loss due to the amplifiers can be no more than 3 to 4 dB at the upper frequencies. The plot in ***Figure 4*** shows a FFT of a 198 MHz input signal buffered by a wide bandwidth differential output amplifier and sampled by an 8-bit ADC at 500 MSPS. The plot shows the amplifier has very low 2nd and 3rd harmonic distortion at this frequency and enables the ADC to capture signals with noise and distortion figures that are comparable to the performance obtained from a dedicated AC-coupled signal path.

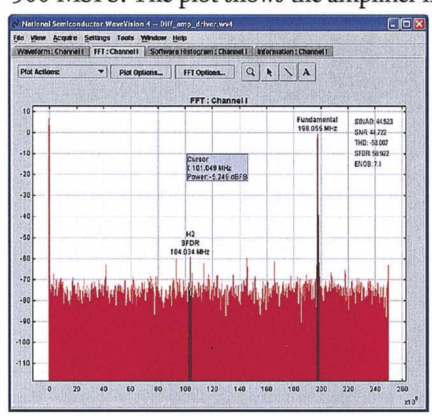


Figure 4. FFT Plot of a 198 MHz Sine Wave Sourced by a High-Speed Differential Output Op Amp, Sampled at 500 MSPS by the ADC08D500

Summary

Amplifier performance is continually being enhanced to deliver increased bandwidth and lower THD. With ADCs pushing well into the GSPS range, complimentary amplifiers that can interface to these converters will be in demand. Not only will system cost be reduced by eliminating circuit paths, the performance of the system will not be compromised and will allow designers to offer higher performance for lower cost, while reducing design time for front-end electronics. ■

The design of a differential output amplifier circuit was extensively covered in Signal Path Designer℠ #101, *A Walk Along the Signal Path*, available at **signalpath.national.com/designer**

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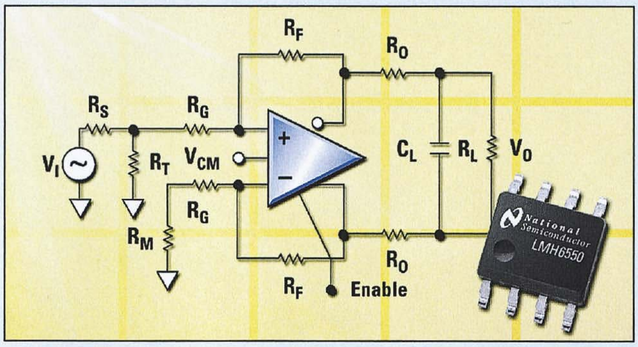


Differential, High-Speed Op Amp

The LMH6550 is a high-performance voltage feedback differential amplifier. The fully differential topology allows balanced inputs to the ADCs and can be used as single-ended-to-differential or used as differential-to-differential. This amplifier has the high speed and low distortion necessary for driving high performance ADCs as well as the current handling capability to drive signals over balanced transmission lines such as CAT-5 data cables. The LMH6550 can handle a wide range of video and data formats.

With external gain set resistors, the LMH6550 can be used at any desired gain. Gain flexibility coupled with high speed makes this device suitable for use as an IF amplifier in high performance communications equipment.

Features

- 400 MHz, -3 dB Bandwidth (V_{OUT} = 0.5 V_{PP})
- 90 MHz, 0.1 dB Bandwidth
- -92/-103 dB HD2/HD3 at 5 MHz
- 3000 V/μs Slew rate
- -68 dB Balance error (V_{OUT} = 1.0 V_{PP}, 10 MHz)
- 10 ns Shutdown/enable

The LMH6550 is ideal for use in applications requiring a differential A/D driver, video twisted pair, differential line driver, single end-to-differential converter, high-speed differential signaling, IF/RF amplifiers, or SAW filter buffer/drivers. It is available in the space-saving SOIC-8 and MSOP-8 packaging.

www.national.com/pf/LM/LMH6550.html

High-Performance, Low-Power, Dual 8-Bit, 500 MSPS A/D Converter

The ADC08D500 is the industry's lowest power dual 8-bit 500 MSPS analog-to-digital converter. It simultaneously digitizes two signals to 8-bit resolution at sampling rates up to 500 MSPS or one signal at sampling rates up to 1 GSPS. Consuming a typical 1.4W at 500 MSPS from a single 1.9V supply, this device is guaranteed to have no missing codes over the full operating temperature range. Its best-in-class dynamic performance, linearity, and pulse response make it ideal for data acquisition systems. The low power consumption allows for small form factors (no heatsinks or fans required) and long battery life.

Features

- 7.5 Effective Number of Bits (ENOB) at Nyquist (typ)
- Bit error rate 10^{-18} (typ)
- Single +1.9V (±0.1V) operation
- Interleave mode for 2x sampling rate
- Choice of SDR or DDR output clocking
- Multiple ADC synchronization capability
- Serial interface for extended control
- Fine adjustment of input full-scale range and offset

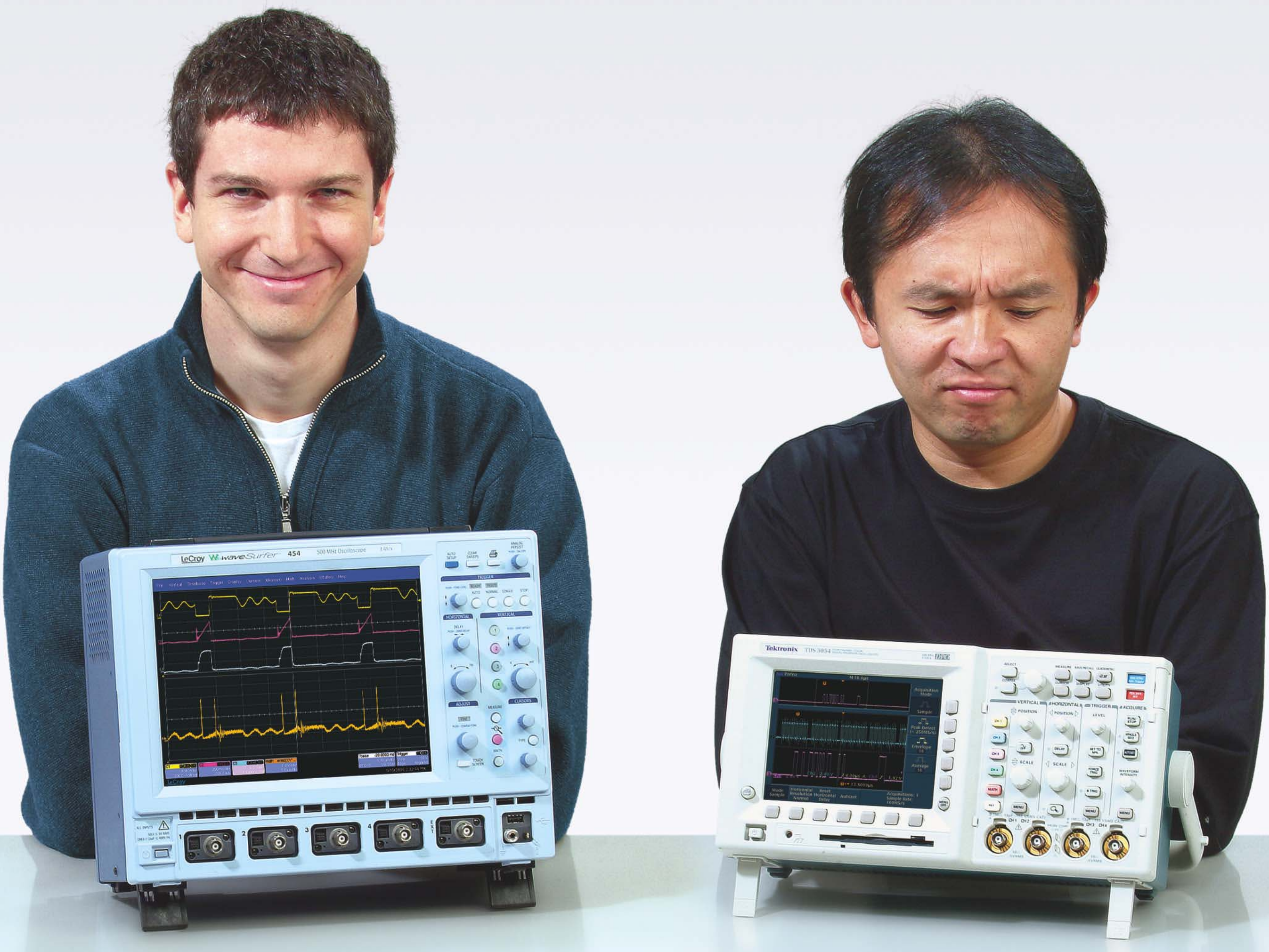
The ADC08D500 is ideal for use in direct RF down conversion, digital oscilloscopes, satellite set-top boxes, communications systems, and test instrumentation. This A/D converter is available in a thermally-enhanced exposed pad LQFP-128 and operates over the industrial (-40°C to +85°C) temperature range.

www.national.com/pf/DC/ADC08D500.html

National Semiconductor

570102-029

Wow! Why?



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100X longer capture time
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http://www.lecroy.com/goto/WaveSurferAd

Embedded computer features conductive cooling

The new seven-slot, 3U Hercules CompactPCI system from Inova Computers features a special aluminum heat sink that conducts heat away from the CPU and peripherals. This thermal-management scheme prevents hot spots inside the chassis and extends system MTBF. Running Windows XP Embedded, Hercules comes with a CPU board with either a 1-GHz Celeron M or a 1.4-GHz Pentium M, an intelligent power-supply-unit board, and five vacant backplane slots for adding CompactPCI I/O and controller boards for such functions as digital video, global positioning, wireless LAN, and removable hard-disk drive.

The rugged Hercules computer system delivers a CPU and intelligent power supply in a conduction-cooled, seven-slot CompactPCI chassis.

The CPU board contains a Phoenix BIOS; 256 Mbytes of Compact Flash memory; a USB 2.0 port; a Fast or Gigabit Ethernet port; a 2048×1536-pixel analog video accelerator; and three 24V, optoisolated digital I/O lines. The system has a standard −20 to +50°C operating-temperature range plus an optional −40 to +85°C range. A board-support package provides utilities to monitor the operating parameters of the system and maintain reliability. Prices begin at $1675 (OEM quantities), and delivery is four to eight weeks after receipt of order.**—by Warren Webb**

▷**Inova Computers**, www.inova-computers.com.

FEEDBACK LOOP

"Consider how a youngster might think about it: 'Why should I blow four to eight years in college fighting for one of a steadily declining number of engineering jobs that are all getting sent overseas anyway?'"

Bruce Lane, in *EDN*'s Feedback Loop, at www.edn.com/article/CA6280033. Add your comments.

Class D makes audio chip Grade A

Available in a 4×4-mm package, the LM4935 audio chip provides a complete subsystem for smart phones and VOIP (voice-over-Internet Protocol) handsets. The device handles many common analog and digital input and output formats and includes a Class D speaker amplifier that delivers 570 mW into an 8Ω load.

Flexibility is the LM4935's hallmark. It can accept digital-audio data in PCM (pulse-code-modulation) format over a bidirectional I^2S or I^2C digital link. For analog input signals, built-in switching and mixing circuitry allows the device to accept a stereo signal, two separate mono signals, differential mono signals from a cell-phone-radio module, and internal or external microphones. The output lines support OCL (output-capacitor-less) or ac-coupled drives of 30 mW into a 32Ω load, an earpiece amplifier, and a line output for an external amplifier. Other features include a SAR (successive-approximation-register) ADC for system monitoring and a high-fidelity DAC.

The device comes in a 49-bump micro-SMD package with 0.5-mm pitch and costs $3.95 (1000). National Semiconductor also offers online design tools at http://wbench.national.com and seminars at its main Web site.

—by Richard A Quinnell, Contributing Editor

▷**National Semiconductor**, www.national.com.

Driver handles three-phase brushless motors

The high cost of electronic control for BLDC (brushless-dc) motors has long been one of the barriers to their use in system designs. Now, Apex Microtechnology is offering a low-cost motor-driver IC to remove that barrier for users of three-phase BLDC motors requiring currents as great as 5A per phase. The company's SA305 combines drive transistors with logic control, current sensing, and fault-protective circuits to simplify design-in. The device's high switching speed and driver power efficiency help reduce manufacturing costs.

The term "motor driver" does not quite do the SA305 justice; the term "intelligent switching amplifier" seems more accurate. The device offers three independent drive channels that can each source or sink current on an output line based on digital signals coming from a DSP or a microcontroller that controls the SA305. The device is not simply a passive driver, however. It has built-in circuitry to prevent simultaneous "source" and "sink" drive signals from creating an internal short circuit. Instead, the SA305 automatically inserts dead time to one drive command if the other drive command is still active. This feature prevents shoot-through-current situations from damaging the drive transistors.

Other built-in safety features include junction-temperature sensing and output-short-circuit protection. If the junctions of the drive transistors reach 160°C, the device shuts off the drive transistors and asserts the fault line. A short circuit across output pins has the same effect, although designers should mount the device to handle a brief, 500W power surge. An external reset signal restores the device to normal operation. The SA305 can handle continuous currents of 5A and peak currents of 10A, making it suitable for BLDC motors as powerful as ⅓ hp. The drive transistors' channel resistance of less than 0.4Ω and PWM-controlled drive current (switching at 100 kHz) mean that the device generates little heat. This feature allows the device to operate with limited or no heat-sinking, reducing implementation costs.

You can independently control the output transistors for the three channels, which means that the SA305 is not limited to motor applications, according to Apex's vice president of engineering, Tom Price. The unit can just as easily handle relays, lighting, and other high-current loads. The SA305 comes in an SIP with a grounded heat tab. The price is $13.10 (10,000).

—by Richard A Quinnell, Contributing Editor

▷**Apex Microtechnology Corp**, www.apexmicrotech.com.

The SA305 motor-driver IC combines drive transistors with logic control, current sensing, and fault-protective circuits to simplify design-in.

DILBERT *By Scott Adams*

Supply controls LED-light levels

The LTC3783 current-mode multitopology converter drives high-power-LED strings and clusters. The device provides constant-current PWM (pulse-width-modulated) power to control the brightness level of the LEDs. It can achieve a dimming ratio of 3000-to-1 using digital methods and 100-to-1 using analog control. The device also offers a dimming mode that guarantees the color integrity of white and RGB LEDs.

This controller can operate in boost, buck, buck-boost, SEPIC (single-ended primary-inductance-converter), and flyback-converter modes. It can also operate as a constant-current/constant-voltage regulator without a current-sense resistor.

The LTC3783 can accept input voltages of 3 to 36V and provides overvoltage protection. It integrates drivers for power and load MOSFET switches and 20-kHz to 1-MHz switches based on a single frequency-setting resistor. Price is $2.85 (1000).

—by Richard A Quinnell, Contributing Editor

▶**Linear Technology Corp**, www.linear.com.

This LED-power-driver device offers design flexibility and color stability over a 3000-to-1 dimming range.

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Now that DaVinci products are here, your digital video innovations are everywhere.

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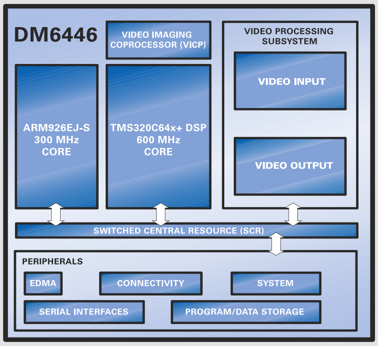
Processors: Digital Video SoCs:

- TMS320DM6446 – Video encode/decode
- TMS320DM6443 – Video decode



Performance Benchmarks:

STANDALONE CODECS	DM6446	DM6443
MPEG-2 MP ML Decode	1080i+ (60 fields /30 frames)	720p+
MPEG-2 MP ML Encode	D1+	n/a
MPEG-4 SP Decode	720p+	720p+
MPEG-4 SP Encode	720p+	n/a
VC1/WMV 9 Decode	720p+	720p+
VC1/WMV 9 Encode	D1+	n/a
H.264 (Baseline) Decode	D1+	D1+
H.264 (Baseline) Encode	D1+	n/a
H.264 (Main Profile) Decode	D1+	D1+

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  - G.728
  - G.723.1
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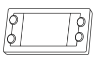
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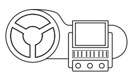
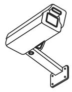

Automotive Infotainment


Digital Still Camera


Digital Video Innovations


Video Surveillance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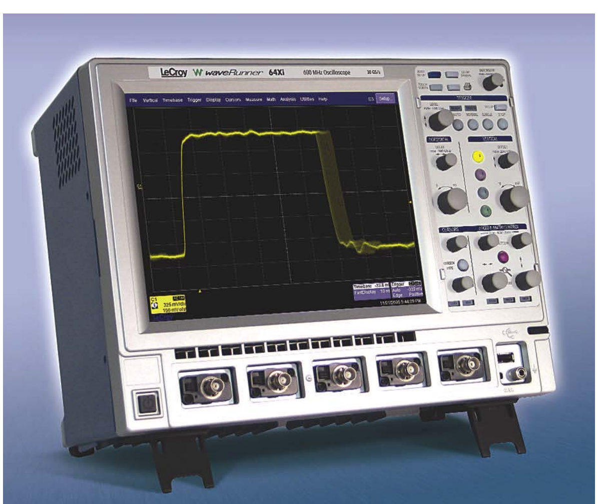
Scopes combine big displays, small footprint

With its WaveRunner Xi line, LeCroy brings big-scope performance and a 10.4-in. touch-sensitive display to a package whose benchtop footprint is no larger than that of scopes that offer much lower performance. What's more, the units achieve this goal at base prices of $7500 to $11,000. Like the lower cost WaveSurfer, WaveRunner Xi scopes measure only 6 in. deep. Whereas the footprint is one-third to one-half that of most other instruments in this class, the display is 1.5 and 2.5 times that of 8.4- and 6.4-in. screens, respectively.

The scopes offer sampling rates as high as 10G samples/sec on the 600-MHz unit with pairs of channels interleaved and have standard 2M-point/channel memory; as many as 24M points/channel interleaved are optional. The high sampling rates, providing at least 10× oversampling, result in excellent signal fidelity on fast edges and high-frequency signals and ensure accurate timing measurements when all channels are active. These sampling rates exceed those of most higher priced competitive scopes having bandwidths of 1 or 1.5 GHz. In addition, LeCroy offers the MS-32 mixed-signal option, which allows users to add to a four-channel WaveRunner Xi 32 digital logic-timing-analysis channels, each with 1M points/channel (32M points total). This feature expands the four-channel scope to four analog and 32 digital channels and significantly enhances mixed-signal and embedded-controller debugging.

The WaveStream fast-viewing mode provides brightness-graded intensity with a decay time similar to that of the phosphor on an analog screen. This mode operates to 10G samples/sec with update rates to 8000 waveforms/sec for improved capture of higher frequency abnormal events.



WaveRunner Xi scopes provide the performance of larger and costlier instruments in a 6-in.-deep package with an 800×600-pixel, 10.4-in. screen.

The WaveRunner Xi-series scopes are available in 400- and 600-MHz bandwidths. The 400-MHz unit comes with four channels, and the 600-MHz units are available with two or four channels. All models sample at 5G samples/sec on all channels simultaneously, and the 600-MHz model interleaves to 10G samples/sec. All models provide memory of 2M points/channel or 4M points/channel, interleaved, which equates to a 400-µsec capture time at the full sample rate. Memory as deep as 12M points/channel or 24M points/channel interleaved is optional.**—by Dan Strassberg**

▷**LeCroy Corp**, www.lecroy.com.

01.19.06

UWB-chip-set maker preps rollout of consumer products

You've been hearing about UWB (ultrawideband) technology for seemingly a decade while waiting for products to appear. Most pundits blame the standards impasse on the IEEE 802.15 committee. However, Matthew Shoemake, president and chief executive officer of start-up WiQuest, disagrees. Shoemake claims that it's simply taken a couple of years for the WiMedia group to finish a spec and for semiconductor companies to, in turn, deliver products. Shoemake doesn't seem bothered a bit by the lack of an industry standard or that the rival UWB Forum (www.uwbforum.org) group is headed down a different path, as his company launches the Gigabit WQST110 baseband and PHY (physical)-layer chip.

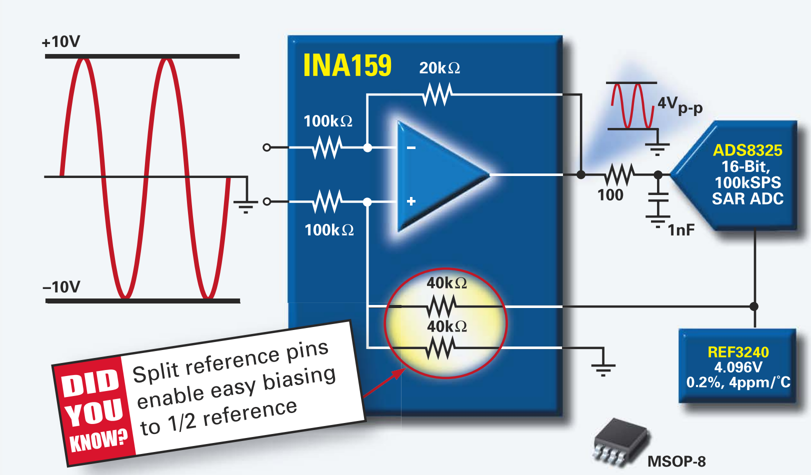
WiQuest joins Alereon (www.alereon.com), which launched a WiMedia chip in October 2005 (see "Chip family offers WiMedia/UWB compliance," www.edn.com/article/CA6275575), with products that can enable applications such as UWB printers, cameras, and media players. The WiQuest differentiator comes in the fact that it offers a 1-Gbps data rate. The WiMedia spec defines a maximum rate of 480 Mbps.

Shoemake claims that the WiQuest offering will maintain compatibility with other WiMedia chips and offer significantly higher performance when two WiQuest-based products connect on a UWB network. He argues that the speed provides the reason for UWB to exist. The Gigabit rates provide a reason for product designers to use UWB either in place of or alongside 802.11 chips that feature much longer range–and certainly instead of UWB Forum technology that, according to Shoemake, will be limited to rates of approximately 100 Mbps.

The company pledges to have consumer products on shelves by the third quarter. Samples of the chips and a $15,000 development kit are now available. WiQuest claims the BOM (bill-of-materials) cost for an add-on UWB module for a PC will be approximately $20 (medium volumes).—by Maury Wright

▶**WiQuest Communications, www.wiquest.com.**

Connect ±10V Signals to Single-Supply ADCs



Burr-Brown Products from Texas Instruments

▶ Applications

- Differential to single-ended conversion
- Industrial process control
- Data acquisition
- Test equipment
- Instrumentation

▶ Features

- Gain of 0.2 ±0.02% (max)
- Low offset: ±100µV
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- Wide bandwidth: 1.5MHz
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Precision Level-Shifting Difference Amplifier

The new **INA159** is a unique, level-shifting difference amplifier with a gain of 0.2. Designed to simply and accurately interface ±10V signals to single-supply ADCs, INA159 is particularly well-suited to applications with 4.096V and 5V references. It also is designed to drive 16-bit ADCs such as ADS8325, offering a combination of low gain error, high DC precision, excellent AC performance, and low output impedance. **Achieve more:** order your samples today.

Device	Description	Ch.	Gain	Offset (µV) (max)	Offset Drift (µV/°C) (max)	CMRR (dB) (min)	BW (MHz) (typ)	Power Supply (V)	I_Q Per Ch. (mA) (max)	Package	Price
INA159	1.5MHz Precision Level Translation Amp	1	0.2	500	5	86	1.5	1.8 to 5.5	1.4	MSOP-8	$1.59
INA152	Excellent Output Swing	1	1	750	5	86	0.7	+2.7 to +20	0.65	MSOP-8	$1.20
INA132	µPower, High Precision	1	1	250	5	76	0.3	+2.7 to +36	0.185	DIP, SO	$1.40
INA2132	Dual INA132	2	1	250	5	76	0.3	+2.7 to +36	0.185	DIP, SO	$2.35
INA133	High Precision, Fast	1	1	450	5	80	1.5	±2.25 to ±18	1.2	SOIC-8/-14	$1.40
INA2133	Dual INA133	2	1	450	5	80	1.5	±2.25 to ±18	1.2	SOIC-8/-14	$2.35
INA143	High Precision, G = 10 or 0.1	1	10, 0.1	250	3	86	0.15	±2.25 to ±18	1.2	SOIC-8/-14	$1.40
INA2143	Dual INA143	2	10, 0.1	250	3	86	0.15	±2.25 to ±18	1.2	SOIC-8/-14	$2.25
INA157	High Speed, G = 2 or 0.5	1	2, 0.5	500	20	86	4	±4 to ±18	2.9	SOIC-8	$1.40

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Technology for Innovators™ TEXAS INSTRUMENTS

Digital-power controller is fast and software-configurable

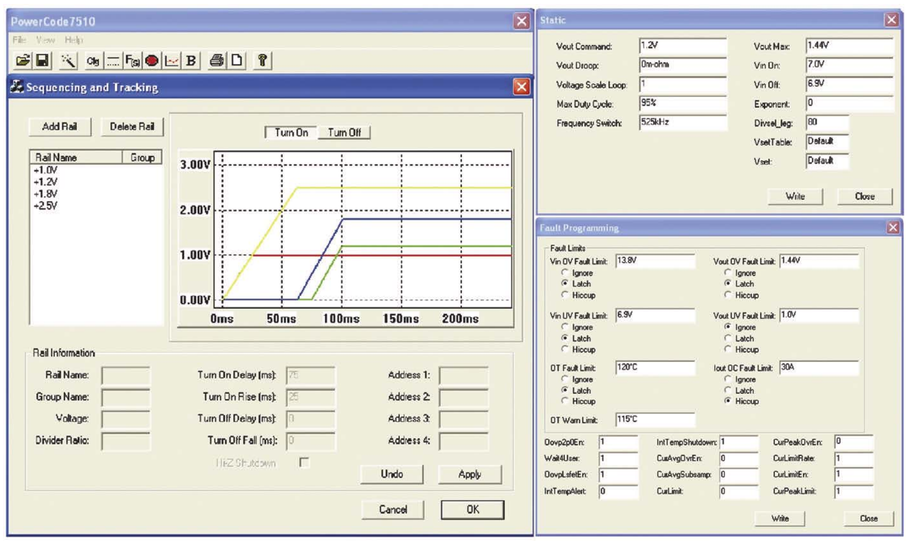
Ron Van Dell, president and chief executive officer of Primarion, likes to preface his introduction of the company's new digital-power-conversion and -management family with a detailed explanation of exactly what "digital power" is—and isn't. "If you put a serial interface on an analog controller, that doesn't make it a digital controller. It's an analog controller with a serial interface. A true digital controller allows you to both configure and communicate with it over an interface and doesn't require any outside hardware changes." With this definition, you must be able to both configure and debug the design through a GUI for the power controller/manager to merit the designation "digital."

Primarion's entry into the growing field of digital-power-management and -control ICs for nonisolated dc/dc converters is the PX7510, which incorporates fast on-chip nonvolatile memory, as well as the industry-standard PMBus to allow software-controlled configuration and real-time system monitoring. The IC's combination of true digital management and nonvolatile memory enables it to allow for less-than-ideal off-chip components and their effect on the control loop. According to Van Dell, this ability breaks the analog paradigm that dictates that overall dc/dc-converter precision can never be better than the precision of the surrounding resistors and capacitors. In addition to external tolerances, the controller can calibrate for other variations, such as drift and aging. This feature allows designs to use lower tolerance, lower cost external components.

The PX7510 operates on a 5V supply and has a frequency-switching range of 150 kHz to 2 MHz. It can share current and thus can adapt from single-phase to a multiphase operation by synchronizing as many as four controllers to balance the power-supply current between phases. The PX7510 is available in an ROHS (reduction-of-hazardous-substances)-compliant, 5×5-mm, 32-lead micro-lead-frame package. Prices start at $1.75 (1000).

—by Margery Conner

▷**Primarion**, www.primarion.com.



The PX7510 allows system configuration, debugging, and communication through its GUI and I²C-based PMBus serial interface and has a frequency-switching range of 150 kHz to 2 MHz.

SOI wafers host higher precision op amps

With its VIP50 process for operational amplifiers, National Semiconductor uses SOI (silicon-on-insulator) structures to build precision amplifiers. The VIP50 has complementary 4-GHz PNP and NPN transistors; a trench that reaches to the silicon dioxide of the SOI wafer electrically isolates each active device. In addition to greatly reduced noise and crosstalk, the structure also eliminates the parasitic transistors that cause latch-up. It can operate at 12V with split supplies for simple biasing. The process supports laser-trimmable precision resistors with closely matched isolated resistors that show no voltage-coefficient effects.

Describing the process as "analog-grade CMOS," National Semiconductor's Erroll Dietz, vice president of the amplifier-product group, notes that it has low 1/f noise, yielding improved accuracy at low frequencies close to dc. "In precision, wideband noise isn't the problem; 1/f noise is the problem," he says. "These transistors perform close to JFET input amplifiers."

National Semiconductor will build several subfamilies of op amps on the process, including ultralow-power chips—amplifiers and comparators—operating from less than 1 μA, precision parts for 2.7 to 12V, and others that will exploit what Dietz says is a tenfold gain in the speed/power ratio. An example is the LMP7711 for instrumentation front ends. With 200-μV offset, it operates as low as 1.8V and offers a CMRR (common-mode rejection ratio) of 95 dB, PSRR (power-supply rejection ratio) of 100 dB, and noise of 7 nV/$\sqrt{\text{Hz}}$ at 400 Hz. Using more than 1 mA, it has a gain-bandwidth product of 17 MHz.

—by Graham Prophet, *EDN Europe*

▷**National Semiconductor**, www.national.com.

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ANALOG DEVICES

VOICES

Altera's John Daane: programmable patriarch

John Daane is president and chief executive officer of FPGA-maker Altera. He is also a former design engineer who worked his way through the ranks at ASIC-maker LSI Logic before taking the helm at Altera. Daane's position and background perfectly suit him to discuss why programmability will gain ground in the consumer and automotive markets and what types of engineers are critical to the task. An excerpt of an interview with him follows. You can find the entire interview at www.reedelectronics.com/electronicnews/article/CA6291917. The complete interview covers Moore's Law, why Altera is hiring, and the global engineering climate.

When you're hiring engineers, what areas of expertise are you looking for?

A As a company, Altera has been hiring more specialty designers.

Define "specialty."

A Analog. When you do high-speed transceivers, you need analog engineers to design the transceivers and a different applications organization to do the verification for different standards. Once you have the transceiver, it can work for PCI Express; it can work for XAUI [10-Gbps attachment-unit interface]; it can work for lots of different standards. You need to characterize that device for different standards, so there's suddenly a whole host of equipment that you have to invest in that you didn't have before.

There are types of engineers for the analog design as well as the applications engineers that have the experience in these different sub-market sets that can do the verification and characterization for you.

Analog engineers traditionally have been the gold standards of engineering because of the amount of experience needed to do the job. Where do you find them?

A That's one of the reasons Altera is investing in engineers in the United States. You find engineers here in areas such as analog and high-density, high-performance-memory design, particularly in advanced geometries, and in a number of areas in which you need experience.

We find we are one of the few companies that is still aggressively hiring in North America. People want to work for a successful, high-growth enterprise. Programmable logic offers a great growth story. This company has been extremely profitable, and a lot of people are excited about the product road map that

we're putting out in front of them. We've had no trouble attracting the talent we want.

One of the complaints–particularly among automotive suppliers–about programmable chips is that the number of defects is higher than in the ASIC world. Is that situation going to change?

A When you look at the core DNA of a company, Altera has always been operationally excellent. We focus on delivering high-quality products on time—much higher quality than any of our competition. We report in our financial statements warranty reserves, and you can see that Altera's warranty provisions are significantly lower than our competition's and our quality is a lot better. Those factors allowed us to extend first into the consumer market, because it has the same concerns about quality as automotive suppliers.

Isn't it a lot different if an MP3 player breaks down from if your car breaks down?

A If you buy a TV and that TV has a failure, you have to take that TV back. You can't send it in the mail because it's too expensive. You have to physically drive it somewhere. So, that problem may turn you off to the brand. Maybe on smaller items that are lower cost and throwaway items, people can live with the fact that it doesn't work well. On a higher end item, which is where you see programmable logic … they are concerned about quality. If we feel we can meet the demands of the consumer industry, we certainly can meet the demands of the automotive industry. The first thing the automotive companies do is to require a packet of information for your products going back many years. That packet includes failure information and quality-reliability information. That's the first thing you have to prove to them before they'll even engage with you—that you have the right quality metrics. You need the systems and procedures in place and the data that back it up.

Is it largely infotainment, or is it the basics of running the car?

A There are some basics, but the opportunity in the next few years is on the infotainment side. Are we in some drive- and power-train applications? The answer is "yes." But the larger dollar opportunity for us is in infotainment.

That's the largest opportunity, anyway, isn't it?

A It's the largest incremental opportunity. If you look at the automotive industry, the number of cars is not going up as a total number. But the electronics is going up, mostly on the infotainment side. If you're supplying microcontrollers that do power-train or engine control, it's a market-share game because the number of cars is basically saturated on a worldwide basis.

–by Ed Sperling, Editor in Chief, *Electronic News*


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GLOBAL DESIGNER

Logarithms: the new floating point?

From the University of Newcastle upon Tyne spin-off Northern Digital comes a microprocessor whose maker claims to be the first to operate directly on numbers that are held in a logarithmic representation. The device targets applications that involve heavy computation loads and would essentially replace today's floating-point processors or coprocessors. Its designers say that it offers a performance gain in such mathematically intensive algorithms.

When designers represent numbers as logarithms, addition or subtraction carries out the multiplying or dividing of two numbers. Clearly, this approach offers the possibility of simplifying the multiplications that lie at the heart of many DSP or graphics algorithms. However, although multiplication and division are simpler, addition and subtraction become correspondingly more complex. According to Northern Digital, although others have considered the concept of a logarithmic processor, no one has thought it worthwhile to implement. By designing a computational architecture that overcomes this problem and efficiently carries out logarithmic addition and subtraction, the company has been able to demonstrate an overall gain in arithmetic performance.

Mathematics usually represents floating-point numbers as 8-bit exponents and 23-bit mantissas. Using the same register space, the equivalent logarithmic representation is an 8-bit integer part plus a 23-bit fractional part. The basic accuracy is the same; however, over the many repeated cycles that characterize computationally intensive tasks, accuracy improves over the floating-point case, because the number of rounding errors involved at each step, which accumulate as a calculation proceeds, decreases.

Northern Digital's processor uses slightly fewer machine cycles to carry out addition and subtraction than a conventional IEEE-754 floating-point unit. But, whereas a floating-point unit might complete a single multiplication or division in 30 or 40 cycles, the logarithmic processor needs only one. This factor underpins the company's assertion that the machine also suits advanced DSP and graphics algorithms: With a four-stage pipeline, the architecture has low latency. In particular, the company says that the design will immediately and efficiently run emerging and experimental DSP algorithms without the effort that is often necessary to tune their code for a conventional floating-point machine.

The company has built a prototype in 0.18-micron CMOS, and this prototype runs at 125 MHz. It is available on an evaluation board that interfaces to a host system through a serial interface, which assembler software and a mathematical-function library backs up. The company is also developing a C compiler. Northern Digital intends to operate as both a fabless semiconductor company and an IP (intellectual-property) source.

—by Graham Prophet, *EDN Europe*

▷**Northern Digital**, www.ncl.ac.uk.

IEEE standardizes SystemVerilog

The IEEE has recently approved the SystemVerilog hardware-description and -verification language as IEEE Standard1800-2005. EDA-tool users in India, particularly those providing design services to clients, see the ratification of this standard as a significant development. "SystemVerilog will help speed up verification of multimillion-gate designs," says GH Rao, vice president of R&D and technology services at HCL Technologies Ltd. "It will also improve the development time of IP [intellectual-property]-based designs, such as SOCs [systems on chips]. We plan to use SystemVerilog from Cadence for verification by the second half of 2006." Rao says that SOC design for multimedia and telecom applications needs standardization of system-level simulation and approval.

"The SystemVerilog standard will provide a great boost to our operations," says Ravi Amur, assistant vice president at the business unit of Hitec at Satyam Computer Services Ltd. SystemVerilog expands language-based electronic design with new and powerful design and verification capabilities based on the Verilog-2005 IEEE Standard1364-2005. Its enhancements include the extension of memory-system tasks for complex memory modeling, operator overloading for simplified expressions, and tagged unions with pattern matching for code conciseness and improved formal analysis.

The main benefits EDA users see from the new standard include improved interoperability between EDA tools from different vendors and unification of methodology for design and verification. Although agreeing with Rao on the design-productivity benefits of SystemVerilog, SN Padmanabhan, vice president of R&D services at MindTree Consulting, cautions, "The design and verification teams will have to learn a newer language and methodology if they want to leverage its full potential." He feels that standardization by itself will guarantee acceptance as a sign-off tool. "Only after many designs [over technology nodes such as 180, 130, 90, and 65 nm] are proved will clients be confident about using this product as a sign-off tool," he says.

—by Chitra Giridhar, *EDN Asia*

▶**HCL Technologies**, www.hcltech.com.
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MIMO delivers range, beam forming delivers video

With the approach of the 2006 rendition of the Consumer Electronics Show (CES), *EDN* decided to take a look at a couple of the latest WLAN wireless-LAN) technologies that purport to carry video. By the time this article hits print, CES will have surely featured a spate of wireless-video demonstrations. The consumer-electronics industry is seeking a "no new wires" way to move compressed digital-video streams, including HDTV streams, around a home. In addition to WLAN approaches, data-over-power-line technology and coaxial cable are challengers in this quest. But the WLAN arena is by far the most active, so *EDN* went into the Digital Den to see how some state-of-the-art WLAN products might perform in a multimedia-centric role. And there is improvement afoot.

As popular as WLAN technology—and more succinctly IEEE 802.11, aka WiFi—is for data networking in the home and office, many believe it will proliferate even more once it starts carrying video in the home. However, even though several *EDN* staffers have been WLAN fans since the 1990s, our tests have consistently found that 802.11 (in all its alphabet soup of flavors) comes up short in terms of range and bandwidth. In fact, although we've applauded the convenience of WiFi, we've also chronicled the fact that a single 802.11 AP (access point) struggles to cover a typical home, even for data networking. And for a network to carry audio or video streams, the gear must perform at a higher level because real-time multimedia carriage can't happen if the WLAN regularly drops, and has to retransmit, packets.

LAY OF THE LAN

Nine months ago or so, I converted my home WLAN to products from Belkin based on Airgo Networks' MIMO (multiple-input, multiple-output) technology. There's some ambiguity at this point as to exactly what qualifies as MIMO. (See **sidebar** "Spatial multiplexing and beam forming" and **Reference 1** for details.) Airgo pioneered a technology called spatial multiplexing, which is one form or element of MIMO, that essentially sends multiple data streams through the same RF channel simultaneously. The technology turns the normally villainous multipath into an asset, presumably delivering greater range and greater bandwidth at a given range.

AT A GLANCE

- The term MIMO (multiple input, multiple output) has come to encompass technologies including spatial multiplexing, beam forming, and smart antennas.
- Tests illustrate that multiple available products can sufficiently cover the home, but data-rate measurement, especially at greater distances, produces varying results.
- Earlier incarnations of 802.11 could not provide video distribution throughout a home, but emerging technologies–some destined to be part of the official 802.11n spec that's in the works–appear ready to succeed in that task.

Belkin's Pre-N product line incorporates spatial multiplexing to increase range, and data rate at a given range, compared with earlier-generation products.

I've tested a number of products over the years, seeking one that offered WLAN coverage throughout my modest 1500-square-foot house and backyard. Ironically, the 900-MHz Proxim Symphony product, operating at a measly 1-Mbps rate, handled the chore back in 1998, but WiFi products failed consistently over the years. When 2.4-GHz 802.11b came along, it boosted rates, but range went down. Then 5-GHz 802.11a boosted rates further, with yet another reduction in range. Finally, 2.4-GHz 802.11g products, and proprietary technology extensions such as channel bonding, began to attack the range issue. Still, I had tested products with the latest chips from Broadcom, Atheros, and others, and never found one WiFi AP that covered my entire property.

The MIMO products, which Belkin initially branded as Pre-N, finally brought me full coverage. Depending on whom you believe, the "Pre-N" moniker either innocently promises MIMO technology today that's similar to what may be in the still-under-development 802.11n spec or misleads consumers into thinking that they are buying an upgradable product.

Regardless, Belkin's products excelled where others hadn't. In earlier experiments, I had moved an AP into a fairly central location in my dining room rather than putting it in the logical place in my office near my cable modem. Yet I had still struggled at times to get a reliable signal on the patio outside the living room. And I had never witnessed a reliable signal in my son's bedroom in the back corner of the house. I hadn't gotten around to measuring the data rate of the link with the Belkin equipment, but the WLAN utility reports "excellent signal strength" everywhere that I've used it. And I even tucked the Belkin router under my desk in my office.

DEPENDING ON WHOM YOU BELIEVE, THE "PRE-N" MONIKER EITHER INNOCENTLY PROMISES MIMO TECHNOLOGY TODAY THAT'S SIMILAR TO WHAT MAY BE IN THE STILL-UNDER-DEVELOPMENT 802.11N SPEC OR MISLEADS CONSUMERS INTO THINKING THAT THEY ARE BUYING AN UPGRADABLE PRODUCT.

NEW NOISE

Enter Ruckus Wireless (formerly, Video 54). A few months back, Ruckus briefed me on its new MIMO technology—in this case, a beam-forming approach branded BeamFlex (**Reference 2**). Ruckus doesn't build 802.11 chips, but rather sells a smart, multiantenna-element front end that dynamically sets antenna configuration and signal paths between sender and receiver to avoid interference. Ruckus also claims to augment the MAC (media-access-controller) layer with a software stack, called SmartCast, that improves multimedia streaming relative to what's in 802.11g and arguably even to what's planned for 802.11n.

Ruckus sent me a pair of products: the MF2900 AP and the MF2501 set-top adapter. The company probably won't sell this pair at retail, hoping a consumer-electronics company or service provider such as a cable company will do so. Ruckus estimates prices of $169 for the AP and $129 for the client. The company bases the products on an Atheros chip set.

I decided to test the Ruckus products


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and also go back and fully evaluate the Belkin products. I connected the Ruckus AP to a 3-GHz Pentium 4 system that I located in my dining room, adjacent to where I'd always performed WLAN-performance tests over the years. I connected the Ruckus client to my 1-GHz Pentium 3 notebook. Fairly quickly, I found that the Ruckus products covered my home just as well as the Belkin products, so I set about to measure data rates.

Many software utilities and other methods exist to measure rates. I relied on a stopwatch and a Windows file transfer for my tests, as I have for all of the WLAN testing that I've done over the years.

With client and AP adjacent, I measured a maximum data rate of 17.8 Mbps. But I ran every test multiple times and the results varied, with one heat coming in at 11.9 Mbps. I suspect that the variation is due to interference over which I had no control. I do know that two other neighbors have WLANs than I can detect from my dining room.

I next went back to my son's bedroom. The distance is around 50 ft, although one never knows how the signal actually travels, whether it's through the walls, bouncing off them on its way down the hall, or the like. I was surprised to measure rates as high as 16.7 Mbps in that location and never saw a rate as low as the minimum rate that I measured with the units adjacent.

Ruckus suggested that I try to add noise to the equation by using a microwave oven. I placed one right next to the AP and set it to work boiling water. I did not witness maximum or minimum performance with the microwave running, but I also could not discern for sure whether this fact was due to the microwave or simply the above-mentioned variation.

Trying to further challenge the Ruckus technology, I took the client outside onto my patio, where I consistently measured rates around 11 Mbps. The range was about 60 to 70 ft, although the signal path may have been clearer than the one to the bedroom. Next, I took the client to the far side of my house on the property line (about 80 ft), where the signal almost surely passed through a stucco wall. There, I measured rates around 9.7 Mbps. The variation in multiple tests became smaller as the data rate dropped.

New WLAN products from Ruckus Wireless employ a beam-forming approach called BeamFlex, along with a MAC (media access controller) embellishment called SmartCast, to provide solid multimedia delivery.

VIDEO FLIGHTS

To test video transmission, Ruckus supplied VLC Media Player, an open-source-software package from VideoLan that you can use to stream video from one PC and decode and play it on another. The company also sent a clip of the movie *Monsters, Inc.*, stored in the DVD MPEG-2 format.

I tested streaming all around the house and yard and never witnessed anything but perfect playback. The microwave had no adverse effect. Following a Ruckus suggestion—that I try a file transfer and a video stream at the same time—I found that video played undisturbed during the file transfer. Moreover, I measured surprisingly fast data transfers at the same time: 10.1 Mbps with the systems adjacent and 7.3 Mbps with the client outside my house on the property line.

Thoroughly impressed, I turned back to the Belkin products. I connected the router directly to the Pentium 3 desktop so that it was no longer connected to my home LAN. And I put the Belkin PC Card in my notebook. With the systems adjacent, I measured rates as fast as 18.8 Mbps, slightly better than the Ruckus performance. Again I witnessed random variation in repetitive tests, with rates

TRYING TO FURTHER CHALLENGE THE RUCKUS TECHNOLOGY, I TOOK THE CLIENT OUTSIDE ONTO MY PATIO, WHERE I CONSISTENTLY MEASURED RATES AROUND 11 MBPS.

dropping as low as 12.9 Mbps.

When I tested the Belkin products at greater distances, however, they did not perform to the Ruckus level. I measured rates in the 13-Mbps range in my son's room and in the 8-Mbps range at my property line, still perfectly acceptable for data networking.

I also used the VLC software to see how the Belkin products stacked up in video streaming. But even with the systems adjacent to one another, I never witnessed perfect video on the client. The playback suffered from dropped frames and occasional blocking artifacts. Apparently there is something to the SmartCast software. The Airgo-based Belkin Pre-N products also include an optional QOS (quality-of-service) feature that is an extension to 802.11g for multimedia, but the Belkin products that I tested can't match the Ruckus on video right now. In fairness, however, a second-generation Airgo chip set is available in products already, and the company has also announced a third-generation IC.

CONCLUSIONS

I had hoped to test the Ruckus link with a high-definition video stream. Unfortunately, I couldn't locate HD content that the VLC software could handle before I ran out of time. When I get a chance to perform that test I will offer an update on our Web site.

For reference, I also tested the data transfer over a wired Ethernet link. With a 100-Mbps Ethernet switch between the two systems, I measured rates as fast as 79.6 Mbps. Clearly, WLANs still have some catching up to do. Belkin advertises its products as capable of 108-Mbps rates, and Ruckus highlights the 54-Mbps 802.11g spec.

For now, I'm sticking with the Belkin products for everyday use; the Ruckus client is a bit unwieldy because it's not in a PC Card form factor. By calling it a "set-top adapter," Ruckus clearly intends the device to be a living-room product, and in that setting, the form factor is fine. Beyond that, it will surely be easier for the company to integrate the technology's six antennal elements into a notebook lid than into a PC Card.

In 2000 I predicted that WLANs would eventually become the A/V network of choice. Subsequently, performance issues with 802.11 forced me to flip-flop and instead pronounce that WLANs would never deliver the needed bandwidth over range. Today, I'm again ready to believe that 802.11n might handle whole-house video. EDN

SPATIAL MULTIPLEXING AND BEAM FORMING

No sooner had we heard the term MIMO (multiple input, multiple output) than it took on multiple meanings.

The term arose out of research at Stanford University, which Airgo Networks was first to commercialize. But as soon as MIMO became a hot term, purveyors of different types of technology latched on as well. Atheros was among the first to use the label on a product that simply had multiple antennas.

In any event, the ambiguous usage has now led to more descriptive technology labels, such as "spatial multiplexing" and "beam forming." Airgo is now using the brand True MIMO to separate the spatial-multiplexing technology that it offers from other technologies that are also being called MIMO.

In spatial multiplexing, multiple signal paths between transmitter and receiver exist simultaneously in the same frequency band, enabled by antenna diversity. This is the technology that will be mandated in the next-generation IEEE 802.11n specification now under development.

But don't dismiss other technologies, such as smart antennas or beam forming, as unimportant. Also called MIMO by some, beam forming can further extend bandwidth over range in spatial-multiplexed wireless LANs. But beam forming will likely be an implementation choice in 802.11n products, as opposed to a requirement.

FOR MORE INFORMATION

Airgo Networks
www.airgonetworks.com

Atheros
www.atheros.com

Belkin
www.belkin.com

Broadcom
www.broadcom.com

Proxim
www.proxim.com

Ruckus Wireless (formerly, Video 54)
www.ruckuswireless.com

VideoLan
www.videolan.org

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- In addition to the references listed above, check out this related article:
  - Double-barreled WiFi test, www.edn.com/article/CA6250011
- Earlier experiments with WLANs:
  - A man, a LAN, a plan (2004), www.edn.com/article/CA443377
  - Combo, please (2003), www.edn.com/article/CA310391
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Designs that are pearls and designs that are rubbish are there,
And there with the rest are designs that will never be old.

There's circuits from everywhere that triple Es may reside,
And many to count are the abstract and many of use,
And many that seem so attractive they can't be denied,
But few that perform when you build 'em and turn on the juice.

I wish one could know them, I wish there were tokens to tell
Those fortunate circuits that work when you turn on the power;
And then one could publish them freely and not strike a knell
For our firm's reputation for circuit ideas that inspire.

But now you may stare as you like but you cannot devise
Infallible ways to ensure that success be foretold;
They send to the ceiling the smoke of untimely demise
Designs that will die on their bread-boards and never be old.

(With apologies to A. E. Houseman)

This is a parody of one of the poems (XXIII) in Houseman's "A Shropshire Lad."

To learn more on SPICE simulation, Go to: http://rbi.ims.ca/4911-501

Contributing Writer James Bryant has been a European Applications Manager with Analog Devices since 1982. He holds a degree in Physics and Philosophy from the University of Leeds. He is also C.Eng., Eur.Eng., MIEE, and an FBIS. In addition to his passion for engineering, James is a radio ham and holds the call sign G4CLF.

Have a question involving a perplexing or unusual analog problem? Submit your question to:

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PROCESSING OPTIONS

BY ROBERT CRAVOTTA • TECHNICAL EDITOR

CHOOSE THE RIGHT MIX OF PROCESSING TECHNOLOGIES FOR EMBEDDED-SYSTEM DESIGNS.

The number of options for choosing the best processor for embedded-system designs continues to increase. In addition to microprocessors, microcontrollers, and DSPs (digital-signal processors), several unified microprocessors from companies such as Analog Devices, Infineon, Microchip, and Freescale have also emerged (**Reference 1**). These software-programmable devices offer unified-processor architectures that combine features of microcontrollers and DSPs to better mix control and signal processing in a single instruction engine. More recently, new silicon products and more mature tools are available to embedded-system designers to better harness the power of programmable logic as custom accelerators of software algorithms for signal processing (**references 2** and **3**).

The increasing incorporation of digital-signal processing in electronic applications has led over the years to a number of claims and predictions by competing semiconductor providers. One claim is that, for applications with high computational loads, FPGAs are better than DSPs for digital-signal processing and that designers can eliminate the need for DSPs in their designs by adding processor cores in the FPGA. A similar claim for applications that require some signal processing states that a microprocessor architecture that incorporates integrated digital-signal-processing extensions can replace DSPs.

Claims such as these could suggest that FPGAs are encroaching on the domain of DSPs from the computational high end and hybrid microprocessors from the computational low end. However, the replacement of DSPs in embedded-system designs by FPGAs and unified microprocessors is analogous to the bid of 32-bit processors to replace 8-bit processors. In other words, embedded-system designs are


microprocessors
microcontrollers
DSPs
mixed cores
PROCESSORS
FPGAs
custom accelerators
coprocessors
ALU fabrics
soft cores
LOGIC

AT A GLANCE

- The requirements for consumer applications are driving the adoption of mixed-processing designs.
- Each processor option addresses a different sweet spot in the range of processing requirements.
- Software implemented as hardware is a growing opportunity for designers.
- Tools supporting mixed-processing designs need to preserve and incrementally evolve the programming model.

not eliminating the use of DSPs; for analogous reasons, 8- or even 4-bit processors have not become extinct. In fact, the message among semiconductor vendors has been making an important shift over the previous year or two from a position of compete and replace to a stance of coexist and complement. This recent shift is most visible among suppliers of DSPs and FPGAs.

Semiconductor vendors were late in realizing this shift in distinction; their customers understood all along. Different processing architectures best suit different design constraints. As high-volume consumer applications continue to incorporate new features and converge multiple functions into the same end system, designs are employing a mixture of processing architectures in various topologies. A possible positive outcome of this shift from a compete to a complement stance is the eventual availability of development and debugging tools that better simultaneously support mixed-processing options in the same tool.

By mixing heterogeneous processing architectures in the same design, developers can lower the system cost, power consumption, design complexity, and time to market. A mixed topology can also afford a development team a simpler maintenance environment that supports a shorter development time between iterative and derivative design cycles. This situation is possible because each type of processing architecture supports a different sweet spot in the spectrum of processing requirements (see **sidebar** "Processing sweet spots").

SWEET SPOTS

General-purpose microprocessors trade off cost and power efficiency to maximize and deliver high processing performance and the most flexibility of all the processor architectures. To achieve the highest processing performance in the face of uncertain processing behavior, microprocessors often employ additional complexity in their circuitry to offset the impact of unpredictable changes. This additional circuit complexity can take the form of superscalar architectures with deep pipelines, multiple levels of on- and off-chip cache memory, branch-predic-

PROCESSING SWEET SPOTS

Each type of processing architecture fits a sweet spot from the total range of processing complexity (Figure A). All of the sweet spots overlap other sweet spots to provide full coverage of the possible processing scenarios. The assumption is that, if the field of possibility contains any uncovered space, an alternative specialized architecture would exist. As application requirements further push the processing requirements on the right of the processing spectrum of the computational load, you see the introduction of unified and then mixed-processing topologies.

In looking at how to evaluate software complexity, this article identifies four measurements of processing. The computational load is a measure of the number of repetitive computations the application needs to perform over a period of time. With the computational load, the control processing for the computations helps indicate when a multistate algorithm would become too large as a pure hardware implementation. This article uses these two measurements as the primary axes for mapping the processor sweet spots.

Application processing is analogous to computational load; however, the code does not repeat consistently and predictably. Application processing is code that would not lend itself to a parallel implementation. Last is the measure of the system's response requirements. Of most interest are the response requirements for real-time systems. This measure helps identify when the timing uncertainty in program execution—possibly from the operating system or from using a cache—would exceed an application's response requirements. It also helps identify the key application requirements that microcontrollers fill.

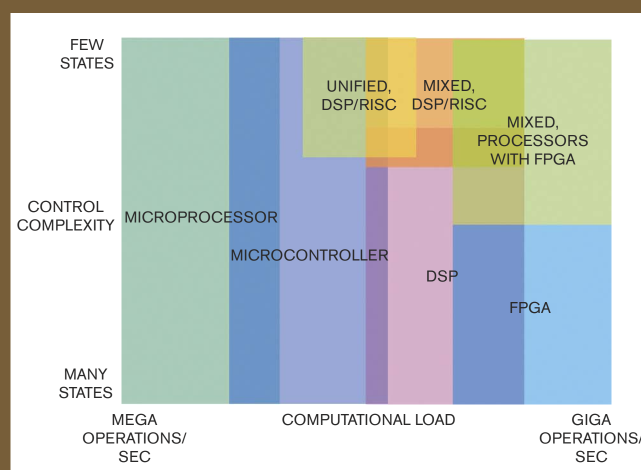

Figure A A conceptual mapping shows how the sweet spots of processing architectures can complement each other to cover the range of an application's processing requirements (assistance from Gary Banta, chief executive officer of Stretch).

tion logic, multiple-instruction-issue engines, out-of-order execution, and speculative execution.

To maintain the highest level of flexibility, microprocessors rely on external memory, devices, and controllers to interact with the real world. They can run large, complex operating systems and receive support from a mature development-tool infrastructure that enables significant reuse of legacy software. Microprocessor-based systems are ideal for quick and dirty rapid prototyping and proof-of-concept exploration in which cost, power consumption, and system size can take a back seat to a shorter development cycle. An example of this situation is evident in the choice of processors for most of the entries in the DARPA (Defense Advanced Research Products Agency) Grand Challenge (**Reference 4**).

The processing sweet spot for general-purpose microprocessors is to support systems that exhibit high uncertainty in processing behavior and loads, such as when executing, managing, and multitasking disparate processing threads over the same processor resources. Desktop and handheld computers are common examples of these systems. The flexibility of microprocessors enables them to most easily support the development of user interfaces and high-level application code.

Microprocessors are available commercially in dozens of configurations. Common microprocessor architectures include x86, ARM, MIPS, and PowerPC, and each architecture can rely on support from a number of suppliers. In contrast, microcontrollers are available as dozens of architectures and in device configurations that number in the thousands. (**Reference 5** lists dozens of microcontroller suppliers and the devices they offer.)

Microcontrollers are specialized processors that trade away the flexibility and general processing performance of microprocessors to gain an advantage in cost and power efficiency. They accomplish this feat by delivering single device configurations that optimize on-chip resources to best meet the needs of their target applications. Each device integrates a processor core with on-chip memory, timers, I/O lines, and appropriate peripherals and device controllers. Examples of on-chip peripherals include ADCs; DACs; PWMs; and serial-communication interfaces, such as I^2C, SPI, and UARTs. In general, microcontrollers are self-contained processing and control systems that require significantly fewer external components than microprocessors to operate.

RTOSs have fewer features than microprocessor operating systems, so they can better support deterministic system operation.

Microcontroller suppliers differentiate their products through features such as processing performance, integrated peripheral sets, on-chip memories, memory management, packaging options, power management, and development support. A single microcontroller family often comprises many similar and derivative configurations that offer designers a range of prices for varying amounts of processing and on-chip-resource support. Microcontrollers are more cost-efficient but less flexible than general-purpose microprocessors because they optimize board space, code size, and power dissipation for their target embedded-system applications.

Another difference between microcontrollers and microprocessors is the level of abstraction of the available resources they present to designers to better meet the constraints of real-time processing. Whereas designers using microprocessors usually rely on richly featured operating systems to abstract and manage the peripheral resources, designers using microcontrollers access the on-chip peripheral and controller resources directly or through homespun or commercially available RTOSs. RTOSs have fewer features than microprocessor operating systems, so they can better support deterministic system operation.

The processing sweet spots for microcontrollers are systems that need to be able to deterministically respond to external real-world events, such as for machine and motor control, with tight latency tolerances. Microcontrollers are capable of rapid, frequent, and prioritized context switching. Many employ specialized hardware-interrupt processing that enables the system to sense and react to external events within a few clock cycles to provide a small and deterministic response window appropriate for real-time control applications. This fast, deterministic interrupt-response capability contrasts with the slower and less deterministic interrupt system of the microprocessor, which may route interrupt handling through the operating system.

Multiprocessor designs offer another emerging sweet spot for microcontrollers. Small microcontrollers, such as 8-bit devices, can operate at the lowest power consumption of all the processor options. These devices are capable of deep-sleep modes that draw extremely low current, and they can wake themselves up based on an external event or an elapsed time. This ability makes them ideal for handling periodic tasks, including health monitoring and system-bring-up sequencing, for systems with aggressive power-consumption targets or that exhibit long periods of idleness. In this case, the small microcontroller can offload these periodic or simple tasks from a larger or more complex processor that would consume more power to perform the tasks.

Similar to microcontrollers, DSPs are specialized processors that trade off the flexibility and general processing performance of microprocessors to gain an advantage in cost and power efficiency. However, DSPs differ from microcontrollers because they sacrifice strength at multitasking or handling context switching for optimizing the on-chip resources

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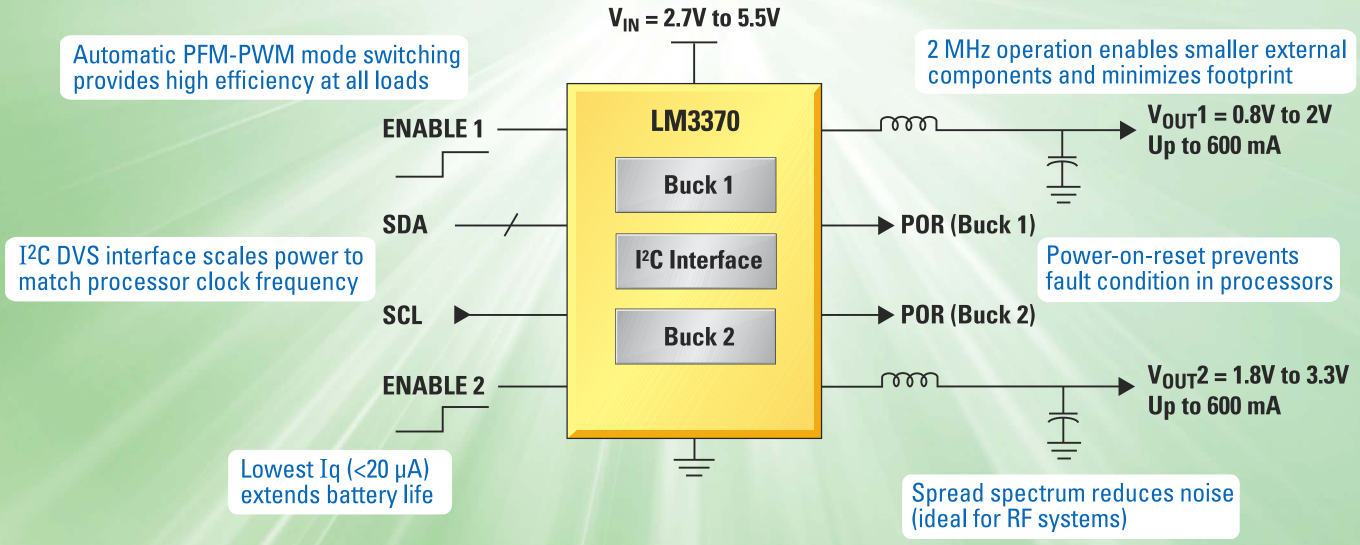

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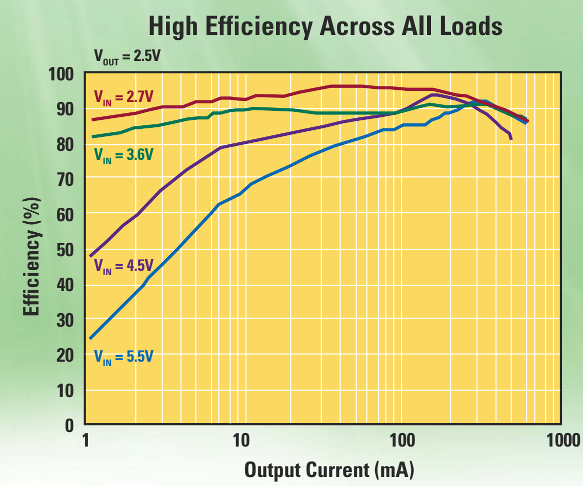

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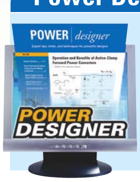

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DSPs support fractional-number types, and they employ specialized address generation for arrays, circular buffers, and bit-reversed algorithms. Their multiple bus and memory structures enable simultaneous memory operations that support single-cycle MAC (multiply-accumulate) execution. Their specialized registers minimize memory accesses and enable zero-overhead looping. The specialized structures that DSPs employ keep the computational units fed with new real-time data. The structures a DSP architecture employs depend on the target application. (**Reference 6** lists DSP suppliers and the devices they offer.)

DSPs differentiate themselves by their sustainable computational performance, code density, power consumption, and development support. Unlike with microprocessors and microcontrollers, signal-processing developers' focus on computational efficiency and on minimizing the amount of context switching in signal-processing applications leads to little or no need for RTOS support. Contemporary DSP architectures employ orthogonal-instruction-set architectures that enable efficient compiler support for most signal-processing code.

The processing sweet spot for DSPs is in delivering high and continuous computational performance at the lowest cost and power consumption. The upper limit of this sweet spot increasingly overlaps with FPGAs, except for highly computational algorithms that include a high level of computational control complexity. VOIP (voice over Internet Protocol) is an example of a computationally intensive algorithm that does not work well as an FPGA-only implementation, because the domain-specific knowledge for compressing VOIP data exhibits too many computational control states and decisions. In the VOIP case, the algorithm implements more cost-effectively as software. The lower limit of this sweet spot overlaps with processors containing unified architectures that combine control and signal-processing structures in a single instruction engine.

Unified-processor architectures are closer to microcontrollers and DSPs than they are to microprocessors. Within a single instruction engine, they either extend microcontroller architectures to add support for signal processing, or they incorporate circuitry to handle control logic to DSP architectures. Unified-processor architectures often support running an RTOS. They are less optimized and specialized than microcontrollers or DSPs, because they must include extra circuitry to bridge the disparate behavior of control and computational processing. Because the same instruction engine does the control and signal processing, it may be easier to more tightly couple the shared data between the two processes.

Because of the general availability of licensable or integrated accelerators, they will decreasingly be a source of differentiation for a design.

The sweet spots for unified-processor architectures are systems with light control or signal-processing requirements, because they can alleviate the need for two heterogeneous processors within the design—lowering the system bill of materials. An advantage of using unified processors in a multiprocessor design is that, even if you partition the processing between the processors as control and signal processing, the designers of both processors are using the same tools; it may be possible to host and port code developed for one processor in the system to the other processor with minimal impact on the development effort.

SOFTWARE AS HARDWARE

Another way to bring processing performance into a design at lower cost or power consumption is by employing application-specific hardware accelerators and coprocessors. Such accelerators may be available as discrete devices or as stand-alone IP (intellectual property) that an FPGA can host. If an accelerator has proved useful for high-volume applications, a processor supplier may integrate it into some of its processor devices; for example, a Texas Instruments DSP integrates the hardware accelerator for the Viterbi decoder. Because of the general availability of licensable or integrated accelerators, they will decreasingly be a source of differentiation for a design. The value in these accelerators is that they offer the opportunity to offload processing capacity to add differentiating features to a system or to reduce the system cost or power consumption.

Last year saw an explosion in the number of tools publicly available to assist developers wanting to accelerate an algorithm in a hardware implementation (**references 2** and **3**). These tools are noteworthy because they enable designers to more easily create custom accelerators or instruction-set extensions. The ability to create custom accelerators can be a longer lasting differentiation, because the acceleration is generally unavailable to the public and may not become a commodity capability as quickly as generally available acceleration IP.

In most cases, these tools target the software-to-hardware implementation to an FPGA. The variety of methods for translating from models, source code, and, in the case of Criticalblue, object code to a hardware implementation suggests that industry participants will in the coming years expend much energy on this form of increasing processing performance. Some of these implementations are fixed-function RTL blocks, and others target a proprietary processor block that the tool configures to optimize the function performance.

The compiler tool from Stretch differs from the other tools because it targets the acceleration to its mixed-processor device, which combines in a single device a processor core with a tightly coupled, programmable fabric that is integrated with the processor pipeline. One goal of the compiler tool is to abstract the pro-

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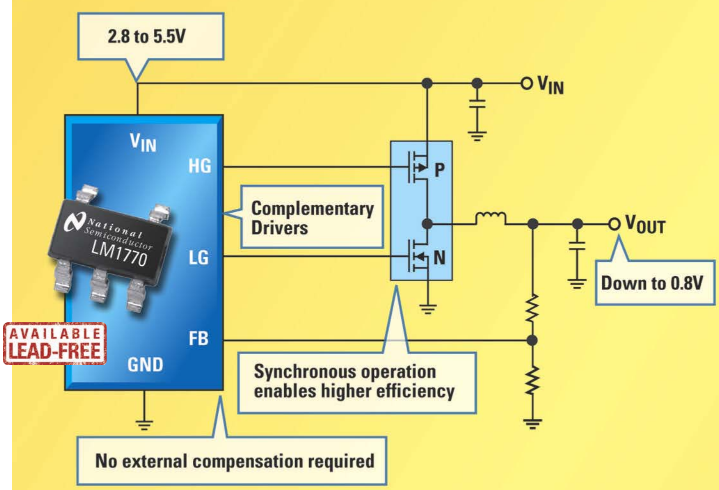
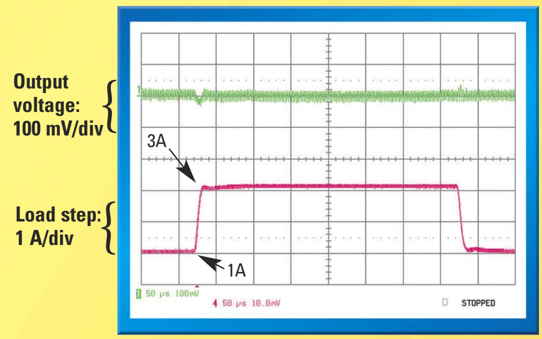
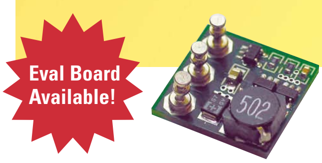


Transient Response



V_{IN}= 5V, V_{OUT}= 3.3V



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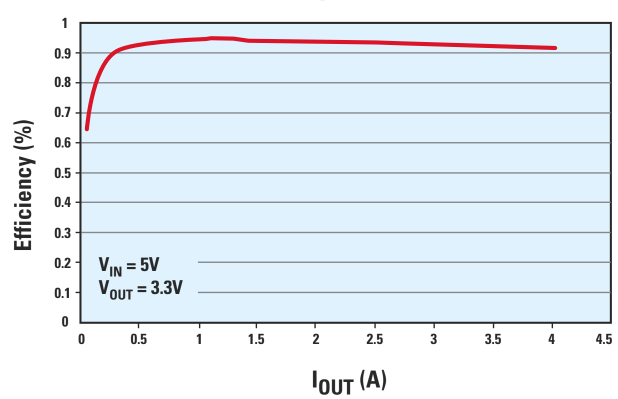

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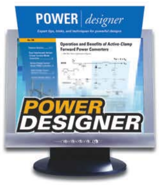

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grammable logic so that the designer can focus on the algorithm and function rather than the implementation. Expect to see a resurgence of mixed-processor devices that integrate both a processor core and an FPGA, most likely with analogous tools to automate the translation of software to hardware.

Linking an FPGA containing an accelerator or coprocessor with a host processor or a DSP is becoming more common in high-performance consumer applications. The falling cost of FPGAs is enabling designers to lower overall design cost and power consumption by offloading the heavy-lifting computations to the FPGA and allowing designers to use a less powerful host processor or DSP. The drop in overall power consumption is possible for applications that can take advantage of the extreme parallelism that an FPGA affords—especially if the FPGA implementation allows the system to use a significantly lower clock rate than it would with a higher performance processor.

Algorithms that exhibit significant parallelism or that you can pipeline to meet tight timing constraints are the processing sweet spots for an FPGA used as a coprocessor to a host processor or DSP. However, in general, the FPGA cannot efficiently replace the entire host processor or DSP from a cost and power perspective, especially in systems that exhibit complex control structures. Recognizing this situation, FPGA suppliers offer proprietary processor cores that the FPGA can host. The tools from the FPGA vendors support configuring the processor core with standard peripherals as well as loosely or tightly coupling a design's custom accelerators with the processor core. In short, the tools are making it easier for designers to use the FPGAs as low-volume SOC (system-on-chip) substitutes.

CHALLENGES

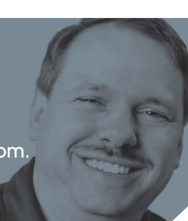
Challenges remain for designers who need to employ a mix of these processing options in their designs. A challenge for the tools that will support mixed-processing designs is how to preserve the programming model and allow designers to exploit the available parallelism. Maintaining a high level of productivity of the development team is essential for the adoption of these mixed-processing options and the tools that support them. It is not uncommon for a design team to exclude candidate processor architectures from consideration because the team lacks experience with the development tools that support them.

A company's legacy code represents a significant amount of engineering and number of lessons learned about the design. Unless the design team is willing to rewrite the application code from scratch, the legacy code will need a repartitioning effort to exploit the available parallelism; however, this effort may be unable to yield clean and natural breaks. Poor repartitioning is analogous to poor data-structure implementation; a data structure that does not naturally and cleanly capture and represent the application requirements leads to troublesome coding and debugging sessions.

Key to preserving the productivity of developers with legacy code and adopting mixed-processing designs is more mature compiler controls. Unless the compiler has full visibility of all of the system resources, it has to make conservative assumptions about resource allocation and usage. To improve compiler performance, new skills are likely to evolve that allow developers to tighten and loosen rules and assumptions that the compiler uses to improve its ability to generate good results from legacy code.

The trend is toward processor suppliers' continuing to provide vertically targeted devices. These devices will integrate an appropriate set of processor resources, hardware accelerators, and programmable logic for target applications, but such devices will exist only for high-volume applications. For all the other applications, designers will have to put together their own mixed-processing configurations. It is becoming clear that using distributed- and multiple-processor topologies is the way to continue the relentless push for more processing performance. The challenge for today's tool providers is to create ways to better encapsulate tasks and implement support for mixed-processor configurations. EDN

You can reach Technical Editor Robert Cravotta at 1-661-296-5096 and rcravotta@edn.com.



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BRIEF

TPS79918 RF LDO Supports Migration to StrataFlash® Embedded Memory (P30)

By Michael Day • Power Management Products/Portable Power DC/DC Applications

Introduction

The Texas Instruments TPS79918 low dropout linear regulator (LDO) provides the required performance to power Intel's new StrataFlash P30 Embedded Memory. Intel is migrating from their 3rd generation 180nm StrataFlash Embedded Memory (J3) to their 4th generation 130nm StrataFlash Embedded Memory (P30). This migration from J3 memory to the P30 memory allows systems to operate at a lower overall current consumption because the P30 V_{CC} voltage requirement has dropped to 1.8 V. Intel Application Note AP812 (document number 306667 Rev 2) recommends using a low dropout linear regulator (LDO) to provide the new 1.8 V voltage rail.

TPS79918 Features

The TPS79918 LDO offers exceptional electrical performance in a small package. It provides a high power-supply rejection ratio (PSRR) greater than 66 dB, low noise, fast start-up, and excellent line and load transient response. It consumes only 40 µA of ground current at full load. No input capacitor is required for operation. The TPS79918 is stable with a small ceramic output capacitor and uses an advanced BiCMOS fabrication process to yield a 110 mV dropout voltage at the full 200 mA output load. Its precision voltage reference and feedback loop achieve a 2% overall accuracy over all load, line, process, and temperature variations. The addition of an optional noise reduction capacitor provides an extremely low noise output voltage. It is fully specified from TJ = –40°C to +125°C and is offered in three packages: ThinSOT23, Wafer Chip-Scale, and 8-pin SON. Figure 1 shows the TPS79918 internal block diagram. The active high enable signal turns the device on after the input voltage goes above the under voltage lockout level (UVLO). UVLO ensures that the input voltage is available, which provides a clean startup waveform. The IC features current limit and thermal shutdown protection in case of a system failure. The internal 500 kΩ resistor along with an external noise reduction capacitor on the NR pin provide an RC filter to reduce the bandgap noise which provides a low-noise output voltage. The quickstart switch initially shorts out this resistor to provide a fast 40 µS startup time. This IC has excellent transient response that is enhanced by the Overshoot Detect circuit which actively pulls the output voltage down during a heavy load to light load transient.

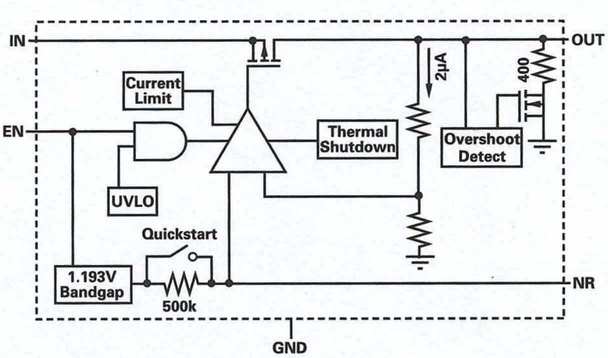


Figure 1: TPS79918 Internal Block Diagram

Intel StrataFlash P30 Embedded Memory Requirements

Migrating existing J3 memory systems to the new P30 memory requires regulating the existing 3.0 V core voltage down to 1.8 V. The 1.8 V core voltage requires regulation within ±0.1 V, which is met by the TPS79918's tight 2% voltage tolerance. The LDO performs well with the load transients caused by rising and falling edges of CE# and OE#. Figure 2 shows that even with a 1 mA to 50 mA load transient, the output voltage only drops 40mV. This performance meets the P30 memory input voltage requirement. Taking system level requirements into consideration, Intel's application note cautions the designer to consider both standby current and active current. Figure 3 shows that unlike some LDOs, the TPS79918's low quiescent current is constant over changes in input voltage and load current. The low quiescent current extends battery life in portable applications. The TPS79918 is available in three packaging options: TSOT-23 (2.9 x 2.8 x 1.0), Wafer Chipscale (WSCP) (1.36 x 1.00 x 0.62), and 2 x 2 SON (2.0 x 2.0 x 0.75), which all meet the P30 active current requirements. The difference between the three packages is size and power dissipation. Assuming a 60°C ambient temperature, the power dissipation for the three packages is 142 mW, 156 mW, and 526 mW respectively. That corresponds to a maximum continuous load current of 119 mA, 130 mA, and 438 mA in this application.

Figure 4 shows the simplicity of a TPS79918 powering a P30 memory module. The only required components are the LDO its self and its output capacitor. The input capacitor is only required if the 3.0 V output capacitor is not located physically near the LDO. The noise reduction capacitor is only needed when powering noise sensitive applications, so it it not required in this application.

Intel specifically recommends the following LDOs for their StrataFlash P30 memory: These four LDOs meet the electrical and temperature requirements for the new P30 memory.

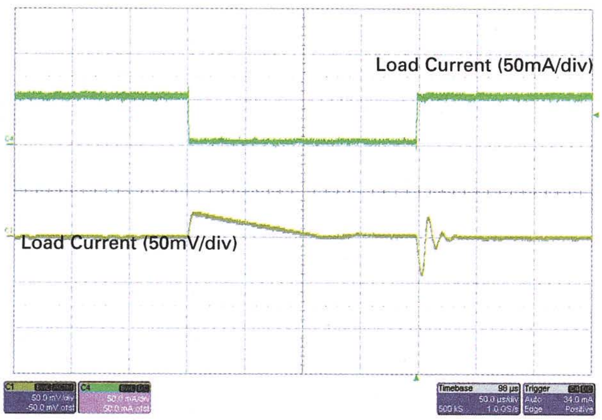


Figure 2: TPS79918 Load Transient

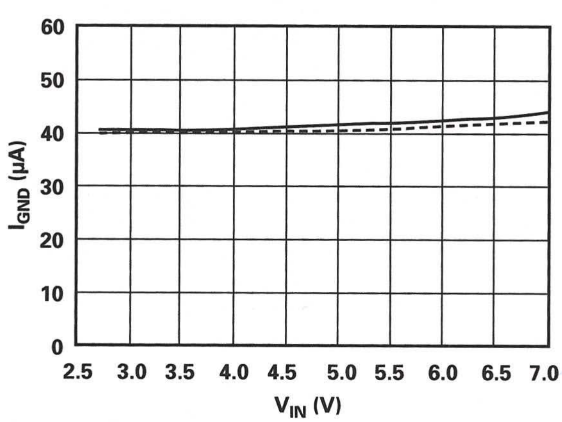


Figure 3: TPS79918 Quiescent Current vs Line and Load

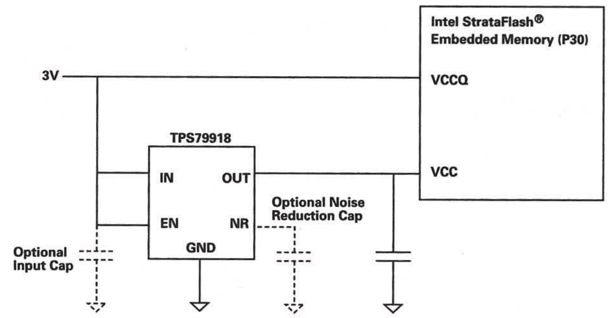


Figure 4: Typical StrataFlash Configuration with LDO

Device	V_O (V)	I_O (mA)	I_Q (µA)	PSRR (dB)	Package	Dimensions (mm)
TPS79918DDC	1.8	200	40	70	TSOT-23	2.9 x 2.8 x 1.0
TPS79918DRV	1.8	200	40	70	2 x 2 SON	2.0 x 2.0 x 0.75
TPS79918YZU	1.8	200	40	70	WSCP	1.36 x 1.00 x 0.62

Conclusions

The TPS79918 LDO from Texas Instruments is ideally suited to power Intel's next generation StrataFlash P30 Embedded Memory. The three packaging options allow the designer to optimize the solution size while the LDO's electrical performance meets the system level requirements for low standby current, transient response, and peak current.

For more information:

Using key word search, download datasheets and other literature at: http://www.ti.com

References:

Intel® Application Note AP812 (Document Number 306667, Rev. 002) available at www.intel.com

Figure 1 Nintendo's latest iterations of its long-running portable-game-console franchise, the Game Boy Advance SP (a), Game Boy Micro (b), and DS (c), square off against Sony's first entry into the category, the PlayStation Portable (d).

BY BRIAN DIPERT • SENIOR TECHNICAL EDITOR

Variations on a theme:

Handheld game systems proliferate, touting varied features and price tags

ENTERTAINMENT CONSOLES ARE GOING MOBILE IN A BIG WAY, FOLLOWING IN THE FOOTSTEPS OF THEIR COMPUTER FORERUNNERS. AT THIS EARLY STAGE IN THE GAME, THERE'S NO SHORTAGE OF OPINIONS ON WHAT DEFINES THE PERFECT SYSTEM, LEADING TO A DIVERSITY OF PRODUCT ALTERNATIVES.

Traditional TV-tethered video consoles are in no danger of obsolescence, but portable counterparts are beginning to supplement and, to a limited degree, supplant them (**Reference 1**). Although mobile units don't directly drive large-screen displays, they don't need to; instead of viewing them from several yards away, players hold them a foot or less from their eyes, and the portable consoles' fine-pitch LCDs deliver lots of detail. They don't hook into a surround-sound speaker system, either, but a set of headphones and sufficient CPU horsepower, which dedicated hardware acceleration often supplements, can deliver an immersive virtual-surround experience (**Reference 2**). And, speaking of CPU horsepower, it, along with graphics muscle, is a fundamental reason for portable consoles' burgeoning success. Potential customers have long appreciated the transportable benefits of a mobile system, but the consoles have only recently become capable of delivering engaging game play, along with high-quality sound and images, while supplying sufficient battery life to justify their "portable" classification.

What characteristics delineate a portable gaming console? That's a tough question to answer; to understand why, look at another rapidly growing mobile-electronics category: the portable computer. Like the portable gaming console, the portable computer has achieved mainstream popularity; look at the computer-store advertisements in your Sunday newspaper if you aren't convinced. Portable computers can finally deliver an adequate amount of storage capacity, processing horsepower, and battery life for the masses. But what's a portable computer? Is it a laptop PC and, if so, in what size, weight, and form factor and with what operating system and application-software

AT A GLANCE

- Price and features define the battle in portable game consoles, just as with living-room-based systems, but, in this case, the added complication of battery life comes into play.
- Nintendo offers a range of systems with various capabilities and prices; the latest DS provides a bridge to the past and a path to the future.
- Sony's PSP (PlayStation Portable) ups the ante on cost but delivers a greater breadth and depth of potential than its Nintendo competitors.
- The Gizmondo and N-Gage are slow out of the gate; did their features not align with consumers' desires, or was their market entry just premature?

suite? Is it a PDA, and, if so, which of the multiplicity of implementation options that currently claim the name "PDA" are valid examples of the portable-computer category, versus being something "lesser," "greater," or "other"? Is a computing-enhanced cell phone or camera—or game console—also a computer?

There's no shortage of opinions regarding what a portable computer is. Similarly, ask 10 people to succinctly define a portable game console, and you'll probably get 10 different answers. This diversity of views reflects the diversity of prod-

(continued on pg 58)

(a) (b) (c) (d)

Figure 2 Nintendo's proprietary NiFi 802.11b-based Layer 3 protocol supports close-proximity player-to-player communication (a) and gaming (b); the DS's recently introduced TCP/IP stack expands the system's multiplayer-gaming capability to a worldwide, Internet-based approach (c) that you can even enjoy for free from the comfort of a nearby fast-food restaurant (d).

TABLE 1 THE HISTORICAL PROGRESSION OF NINTENDO'S GAME BOY LINE

Product	Introduction Date (Japan)	Description
Game Boy	April 21, 1989	Original product, based on Sharp-designed 4.2-MHz Z80 CPU with 160×144-pixel reflective monochrome display
Game Boy Pocket	1996	Smaller and lighter with improved black-and-white display; smaller link port, adopted by all subsequent models until Game Boy Micro
Game Boy Light	1998	Japan-only release added backlit screen to Game Boy Pocket design
Game Boy Color	1998	Color LCD, twice the processor speed, twice as much memory, IR communications port
Game Boy Advance	2001	32-bit, 16.8-MHz ARM processor plus Z80 processor for backward compatibility; 240×160-pixel display
Game Boy Advance SP	2003	Switched to a clamshell design with an internal front light and rechargeable battery; improved backlit screen added in September 2005
Game Boy Micro	2005	4 in. wide, 2 in. tall, less than 1 in. thick. Weighs 2.8 oz. Drops backward compatibility with Game Boy Color and previous titles

UP-AND-COMERS OR WASHOUTS?

The allure of the portable-gaming market is compelling enough that, although Sony's PSP (PlayStation Portable) and Nintendo's product suite currently dominate it, other contenders are also vying for the throne (Figure A). The Gizmondo from Tiger Telematics is one candidate, although it's off to a rough start, having debuted in Europe in mid-March 2005, followed by sales in the United States beginning in late October. From a hardware standpoint, it's a mixed bag in comparison with the DS and PSP. Some would claim that its Samsung-designed single ARM9 CPU leaves it with less processing muscle than the dual-ARM DS, although Gizmondo's ARM9 runs at a much higher, 400-MHz clock rate. Conversely, Gizmondo's Nvidia-developed GoForce 3D 4500 graphics processor, with nearly 1.3 Mbytes' worth of frame-buffer memory, is state-of-the-art.

Gizmondo touts a 2.8-in.-diagonal, 320×240-pixel, color TFT (thin-film-transistor) screen, currently in a 4×3 aspect ratio. However, last summer, *before* the launch of the first-generation unit in the United States, the company indicated that a 16×9-aspect-ratio, wide-screen, second-generation product variant was in the works. Tiger Telematics based Gizmondo on Microsoft's Windows CE. Besides gaming capabilities, it includes multimedia playback, GPS (global-positioning-system) satellite tracking, wireless-Bluetooth PAN (personal-area-network), and GPRS (General Packet Radio Service) WAN (wide-area-network) communications. WAN features include SMS (short-message service), e-mail, WAP (Wireless Application Protocol) browsing, and cellular voice through a Bluetooth headset. Gizmondo also includes a VGA-resolution camera and even a gyroscope that senses and enables applications to respond to the unit's orientation.

The early reviews on the console are lukewarm, the first wave of game titles reportedly isn't engaging or eye-catching, and the battery life is markedly brief. The short battery life is not surprising, considering all of the circuitry the company packed onboard the unit. Tiger Telematics also touts a unique pricing scheme; you can buy a Gizmondo for $229 if you're willing to accept as many as three 40-sec advertisements per day, through GPRS, or $399 with no ads.

Speaking of engaging, no overview of portable gaming systems would be complete without mentioning the Nokia N-Gage series (Reference A). The company in October 2003 introduced the first member of the product family, which it based on a Series 60 phone foundation running Symbian OS Version 6.1 on a 104-MHz ARM CPU with a DSP. Its speaker, microphone, and screen locations made using it as a cellular phone cumbersome: Users needed to remove the unit's battery to swap out game cartridges. The unit's Java-based games were slow and uncompelling, and its multimedia-playback capabilities were limited. Plus, being GSM-only, it couldn't run on CDMA and Japanese cellular networks, a problematic shortcoming given that many game developers are based in Japan.

The follow-on N-Gage QD, which the company unveiled in April 2004, relocated the speaker, microphone, and game-cartridge slot. However, because its developers based it on the same fundamental hardware design as its predecessor, it suffered from many of the same shortcomings. The product family sold approximately 2 million units in 3 years' worth of promotional effort; initial forecasts projected sales of 6 million units in that same time frame. Nokia recently announced that it was suspending further development of the N-Gage hardware platform, although it would continue to offer new games and other software for already-sold consoles, and would consider re-entering the portable-game-console market in 2007 or later. In the meantime, Nokia will focus its efforts on appending gaming functions to its conventional Series 60 cellular handsets.

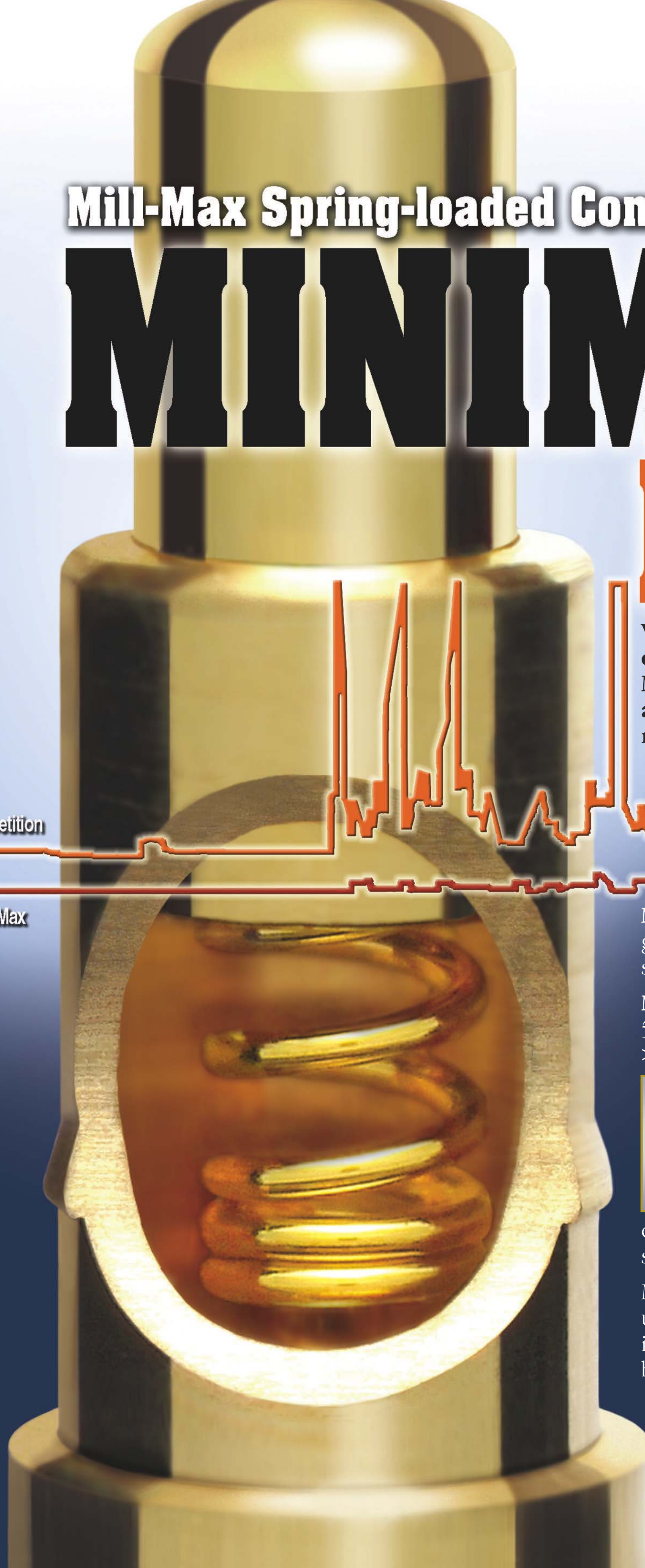
Reference

A **Miller, Matthew, "Phone/game combo fails to engage an audience," *EDN*, Dec 16, 2005, pg 78, www.edn.com/article/CA6290469.**

(a)

(b)

Figure A Tiger Telematics' Gizmondo (a) and Nokia's N-Gage (b) pursue the gaming opportunity from a cellular perspective.



uct offerings now in the marketplace, both from one vendor to another and within each vendor's product portfolio (see **sidebar** "Up-and-comers or washouts?"). For hardware and software suppliers, the $25 billion gaming industry is a gambler's paradise—or, if you prefer, nightmare—fueled by fickle consumers and insistent investors. Guess right, and you're in the pole position for mind-boggling revenue and profits. Guess wrong, on the other hand, and you'll quickly be left in the dust.

Figure 3 The PSP's beefy, multicore CPU and graphics subsystem, along with other enhanced hardware capabilities, deliver highly detailed games (a). The system can also function as a USB mass-storage device and as an audio, still-image, and video player (b). The video-player function employs content streamed over or downloaded from the Internet from a Memory Stick or on a Sony-proprietary UMD optical disc (c).

REIGNING CHAMPION

Nintendo launched its original Game Boy in Japan on April 21, 1989, and in the United States that August (**Reference 3**). Over the subsequent 16-plus years, the company has made steady, calculated improvements to the platform, culminating in today's GBA (Game Boy Advance) SP, which sells for approximately $80, and Game Boy Micro, which sells for approximately $100 (**Figure 1**). The latest Game Boy Micro, which Nintendo unveiled at last May's E3 (Electronic Entertainment Expo) conference (www.e3expo.com), dropped Z80 CPU support and is therefore the first member of the series that's incompatible with original Game Boy, Game Boy Pocket, and Game Boy Color games (**Table 1**).

The Game Boy line is Nintendo's legacy; the Nintendo DS, which, depending on who you talk to, stands for either Dual Screen or Developer's System, in contrast, is the first platform iteration of the company's portable-gaming future (**Reference 4**). Nintendo launched the DS in the United States—one of the rare occasions in which a game device didn't debut in Japan—on Nov 21, 2004, at $149.99; the Japan introduction occurred two weeks later, on Dec 2. Nintendo decreased the price to $129.99 on Aug 21, 2005, and Target stores sold one color variant for $99.99 during the recently concluded 2005 holiday-shopping season. At 5.85 in. wide, 3.33 in. long, 1.13 in. tall (closed), and 9.7 oz, the DS fits into a large pocket. Nintendo included two displays in the DS; both are 3-in.-diagonal with a 4×3 aspect ratio, constructed of a backlit, 0.24-mm-dot-pitch, 256×192-pixel, semitransparent, reflective, TFT (thin-film-transistor), color LCD array. The lower screen incorporates a transparent analog touch sensor, and both screens can display 262,144 colors.

As with the Game Boy Micro, Nintendo also limits the DS' backward compatibility to GBA-targeted titles. The DS contains two ARM CPUs: an ARM946E-S normally operating as fast as 67 MHz but reportedly able to operate as fast as 200 MHz with 8-kbyte-instruction and 4-kbyte-data caches, and an ARM7-TDMI running at 33 MHz but able to operate at 133 MHz with 64 kbytes of internal memory. Nintendo is characteristically coy about its hardware and doesn't discuss the function partitioning between the processor cores; they share 32 kbytes of memory, and the DS also contains 4 Mbytes of system DRAM. The 3-D-graphics engine can transform as many as 4 million geometry vertices/sec, or 120,000 polygons/sec, and it touts a 30 million-pixel/sec fill rate. The DS includes dual speakers, along with a two-channel headphone jack, and it also embeds a microphone for, among other things, voice-recognition applications.

SONY: TOP CONTENDER

After watching Nintendo garner most of the portable-console business for more than a decade, Sony decided to give its living-room-console rival some mobile competition, too. Sony also wanted to give itself a hardware platform to jump-start its media divisions' ambitions by supporting the Memory Stick Duo and 1.8-Gbyte UMD (Universal Media Disc) formats. (Visit the Brian's Brain blog at www.edn.com/briansbrain and read the "Sony versus the hackers" entry for more information.) Sony unveiled the PSP (PlayStation Portable) at the 2003 E3 conference. The company launched the console in Japan on Dec 12, 2004, and in North America on March 24, 2005, although European customers had to wait until Sept 1, 2005, to buy their PSPs. The PSP measures 6.7 in. long, 2.9 in. wide, and 0.9 in. deep; weighs 10.3 oz, including its removable lithium-ion battery and a Memory Stick Duo; and sells for $249.99, including accessories. (Sony sold the device as a stand-alone unit only in Japan for 20,790 yen.) The unit's 4.3-in.-diagonal, 16×9-aspect-

ratio, TFT LCD supports 480×272-pixel resolution and can display 16,777,216 colors. Sony does not specify the display's pixel pitch.

Sony had no backward-compatibility concerns with the PSP, because it was the first in, presumably, a series of portable consoles from the company. However, Sony strove to ease developers' porting of PlayStation 2 games to the PSP, and the distinct PS2 heritage of the PSP's current title suite reflects that simplicity (**Reference 5**). The console contains dual 1.2V MIPS 4KE CPU cores that can operate as fast as 333 MHz but that normally clock no higher than 222 MHz—probably for power-consumption reasons. One core handles most of the system- and game-code processing, and the other, supplemented by 2 Mbytes of embedded DRAM, tackles media processing of audio, still images, video, and the like. The PSP includes 4 Mbytes of embedded DRAM and 32 Mbytes of discrete DRAM.

The PSP's dual-core graphics processor runs at 166 MHz and partitions the graphics pipeline into two classes of tasks: curved-surface and geometry processing on one core and texture-surface and pixel-rendering processing on the other core. Overall specifications, which Sony first revealed at the 2004 IEEE Hot Chips conference at Stanford University, include a peak pixel-fill rate of 664 million pixels/sec and a peak transformed and lit geometry-processing rate of 33 million polygons/sec. Sony also included the reconfigurable-logic-based VME (Virtual Mobile Engine) video- and sound-processing core, which runs at 1.2V and 166 MHz and can implement 3-D virtualization, reverberation, tone control, and other audio-processing functions. Like the DS, the PSP includes left and right speakers and a dual-channel headphone jack, although, in this case, the microphone is an add-on accessory.

WIRELESS VARIETY

The DS and PSP both include WiFi transceivers; the implementation differences lie in the details. Nintendo's design handles only 1- and 2-Mbps WiFi data rates and supports only short-preamble mode. Until recently, it also lacked IP (Internet Protocol) support and, therefore, didn't implement a TCP/IP (Transfer Control Protocol/IP) or UDP/IP (User Datagram Protocol/IP) stack (**Figure 2**). People often refer to Nintendo's proprietary OSI (Open Source Initiative) Layer 3 protocol as NiFi, but that moniker is deceptive. Nintendo implements fully OSI- and 802.11b-compliant Layer 1 physical (wireless) and Layer 2 data-link layer MAC (media-access-control) communications; NiFi's divergence occurs only at Layer 3 and beyond (**Reference 6**).

The discussion about NiFi is now merely academic, though, because Nintendo has just launched its TCP/IP-based Nintendo WiFi network, which you can access through any 802.11b-compatible wireless router or access point. The Nintendo DS doesn't yet offer a Web browser, so networks that require Web-based log-in schemes are normally off-limits, but Nintendo has partnered with Wayport and McDonalds to offer free access in McDonald's US restaurants (see **sidebar** "More at EDN.com"). Other similar wireless-network-access deals are likely to follow.

The PSP, in contrast, implements a full 802.11b-based TCP/IP-network stack at data rates as high as 11 Mbps. It supports both peer-to-peer and infrastructure modes for playing games against other PSP owners both nearby and worldwide. Firmware Version 2.0 added a full-featured Web browser. (Sony previously embedded a limited-function browser within the *WipEout Pure* game.) Version 2.5 firmware included the ability to watch streaming video from the company's LocationFree network-broadcast base station, and Version 2.6 incorporates the ability to access streaming RSS (Rich Site Summary, or Really Simple Syndication) Version 2.0 audio feeds.

The DS and PSP not only support wireless, multiplayer game play, but also claim to support so-called game-sharing mode—that is, the ability to temporarily download a subset of a game to another console's RAM to enable multiplayer mode with someone who doesn't own the game. (Nintendo refers to this feature as single-cartridge/multiplayer.) However, although DS titles widely support game sharing, no PSP titles yet implement it. (The single-cartridge/multiplayer feature extends back to the GBA, although before the existence of the GBA DS, multiplayer mode was possible only through a wired connection between consoles.) The PSP does allow game sharing, however, to download demo versions of games from promotional kiosks to PSPs. (The DS also supports this feature.) At least one PSP title, *Namco Museum*, also supports the download-a-demo-to-another capability, and several PSP titles enable you to download extra postpurchase features, such as *WipEout Pure*'s additional race tracks, features, and soundtracks, from the Internet.

FLEXIBILITY VERSUS PRICE

You might expect that the PSP's greater hardware apportionment and higher price than the DS would translate to not just beefier games, but also broader and deeper features, and you'd be right (**Figure 3**). The console's Internet- and multimedia-related capabilities include audio in WAV (Windows Wave), MP3, AAC (Advanced Audio Compression) within an MP4 wrapper, ATRAC (Adaptive Transform Acoustic Coding) 3plus, and WMA (Windows Media Audio) formats. Both the ATRAC and WMA support are available only without DRM (digital-rights management). The console also supports still images in BMP, GIF, TIFF, and JPEG formats and video in both MPEG-4 Part 2 (Simple Profile) and Part 10 (Main Profile Level 3, also known as MPEG-4 AVC and as H.264) formats.

For complex game-play scenarios, the

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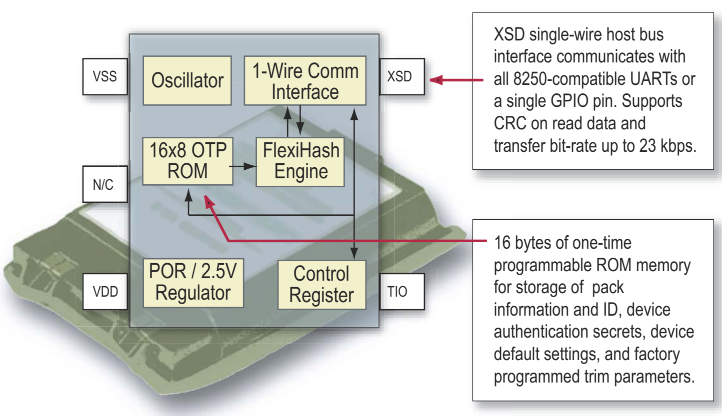
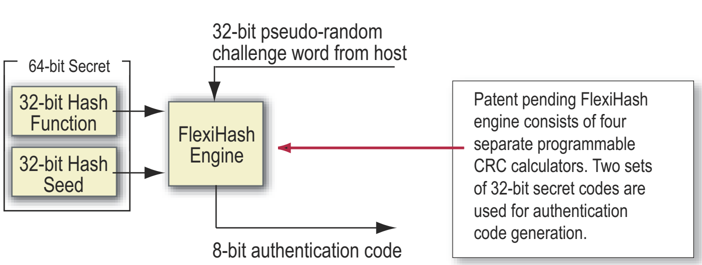
ISL6296 Functional Block Diagram



Device Authentication Process



Key Features:

- Patent pending challenge-response authentication scheme using 32-bit challenge code word and 8-bit authentication code.
- Fast single-step authentication process
- Supports 1-cell Li-Ion/Li-Polymer and 3-cell series NiMH battery packs (2.6V-to-4.8V operation)
- Compatible for use with serial ports offered by all 8250-compatible UARTs or a single GPIO pin
- "Zero Power" sleep mode after bus inactivity time-out period
- 64-bit user-programmable secret for security
- Can also be used in a variety of accessories such as printer ink cartridges where authenticity needs to be verified.
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PSP incorporates more control inputs than does the DS, including an analog joystick. An infrared transceiver supplements the console's WiFi capabilities, and the unit also supports a USB 2.0 wired connection. When you connect the PSP to a computer, a Memory Stick Duo card in the PSP mounts on the computer as an additional drive. The PSP has a more expansive suite of available accessories from both Sony and third parties, reflecting its more comprehensive features. These add-ons include the microphone, protective cases and automobile mounts, amplified speaker-inclusive stands that enable easy viewing of UMD- and Memory Stick Duo-housed movies, extended-life batteries, video-out converters for connecting the PSP to an external display, 3-D-viewing supplements, and adapters that enable the PSP's use of higher-capacity, small-form-factor hard-disk drives through the Memory Stick Duo interface. You can even buy solid-state PVRs (personal video recorders) that record television and dub input videos directly to a Memory Stick Duo in a PSP-resolution-friendly MPEG-4 format for later viewing on your console.

The DS' recent embrace of TCP/IP opens the door to a number of possible expansions of that console's features. The robust artificial-intelligence ability of games such as *Nintendogs* is a testimonial to the system's processing potential. You can view videos on the DS using its Game Boy-compatible cartridge slot and Video Paks from Majesco, although they're of low quality because software running on the CPU decodes them and because of the cartridges' 32-Mbyte capacity. The hardware-accelerated Play-Yan (now Play-Yan Micro) audio (MP3) and video (MPEG-4) adapter, which interfaces to SD cards, is now available only in Japan. The GBA Movie Player third-party adapter mimics the Play-Yan's features and adds e-book support.

Will Nintendo ever offer a Web browser for the DS? Feedback from the company at an early November briefing in Redmond, WA, was contradictory. A public-relations representative indicated that a browser, should it ever appear, would likely come from a third party, but, Reggie Fils-Aime, executive vice president of sales and marketing, later suggested that Web-browser support would be a "provocative idea." He added, "How can we bring new people onboard to buy DS and play DS? Having a Web browser would be highly disruptive. I would love to do it" (**Reference 7**).EDN

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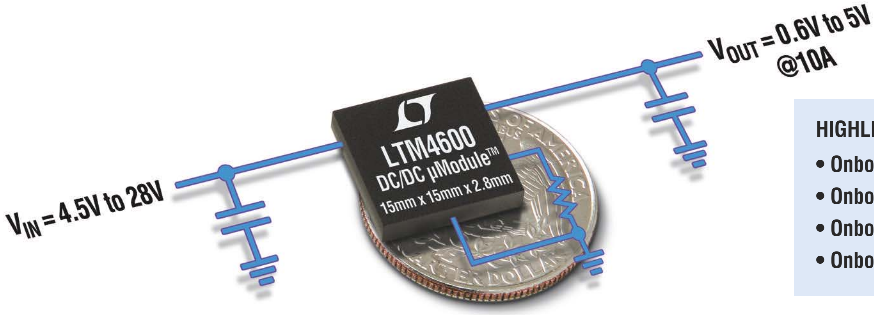
Complete 10A Switchmode DC/DC Power Supply in an IC Form-Factor

High Performance Analog Solutions from Linear Technology

Pre-manufactured DC/DC power supplies, also referred to as point-of-load (POL) modules, have been promising simpler, smaller and quicker solutions. However, they fall short in meeting the demands for system assembly of densely populated embedded boards. Some POL module solutions require an external inductor, many additional input and output capacitors and compensation circuitry. Most are assembled on a small printed circuit board (PCB) and require hand insertion and visual inspection for reliability since the circuit components are exposed and subject to damage.

For heat dissipation and safe component spacing, many embedded systems specify a maximum thickness for components on both the top and bottom of the board. Unfortunately, high power density DC/DC POL modules must implement tall inductors and rely on thick PCBs to alleviate heat dissipation and mechanical stress. In many cases, the large size and tall profile inhibits their use. Therefore, a designer must either design a discrete power supply where it can be optimized to meet the profile requirements or rely on lower power DC/DC modules where thinner inductors are used.

System designers are compelled to make compromises in the selection, performance and definition of the optimum power supply. The ideal solution is a complete power supply with no external power components and easy layout that meets the same surface mount assembly requirements as other digital ICs on the board. The result is a solution that is easy to select, design and assemble.



HIGHLIGHTS
- **Onboard Inductor**
- **Onboard MOSFETs**
- **Onboard DC/DC Controller**
- **Onboard Compensation Circuit**

Figure 1. LTM®4600: Complete 10A Switchmode DC/DC Power Supply

Complete 10A Switchmode DC/DC Power Supply in an IC Form-Factor

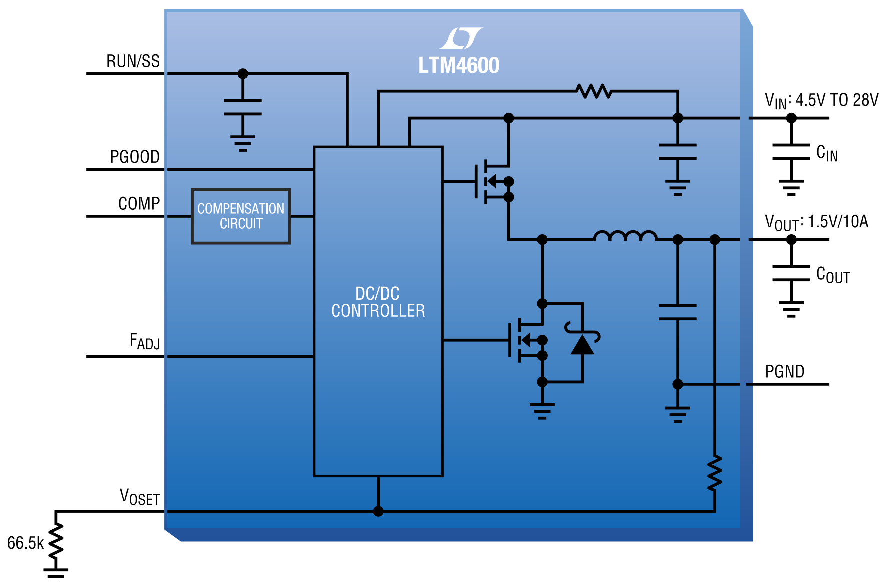


Figure 2. Minimum External Components Required. 1.5V, 10A Application Is Shown

A Complete Power Supply

Figure 1 shows a complete DC/DC power supply solution. This IC-like solution is a 10A synchronous switchmode regulator with built-in inductor, supporting power components and compensation circuitry (see Figure 2 for block diagram). The LTM4600 is a DC/DC µModule™ that meets the spacing and assembly requirements of densely populated and advanced embedded systems. This encapsulated µModule DC/DC power supply is housed in a 15mm x 15mm x 2.8mm LGA package. Its size is smaller than most FPGAs and processors. With a 2.8mm profile and weighing 1.73g, the LTM4600 can be readily placed on the backside of a printed circuit board.

This µModule is rated for both 20V standard and 28V high voltage input operation. The output voltage is adjustable with a single resistor from 0.6V to 5V. The LTM4600 can deliver up to 10A of output current and offers excellent transient response to rapid changes in load currents.

Easy Design Replication by Copying and Pasting the Layout

A common complaint among system designers is the assembly house's alteration of the original layout. The result is many rounds of debugging between the design and the assembly house. This problem is alleviated with the LTM4600.

The simplicity of the LTM4600 minimizes layout errors. Also, the µModule's assembly requires no special tooling.

Excellent Thermal Performance

The LTM4600 µModule has less than 15°C/W of junction-to-ambient thermal resistance. It avoids overheating by dissipating heat efficiently from both the top and bottom of the package. With careful layout, the device's packaging technology permits delivery of 12A load current at 3.3V from a 12V input. For applications with high ambient temperature, the LTM4600 with an optional heatsink and some air flow exhibits exceptionally good thermal performance even at high output power. A detailed application analysis with thermal imaging

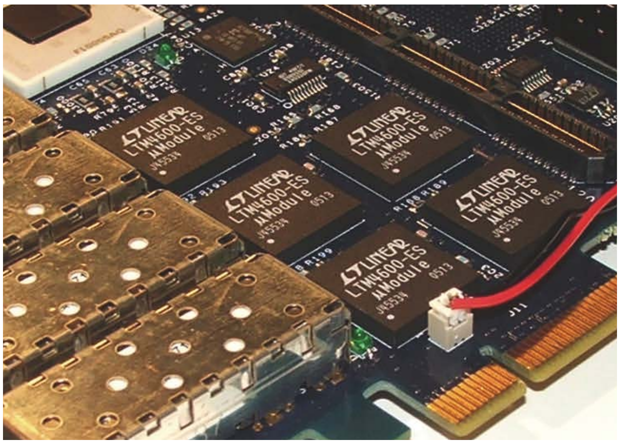


Figure 3. Simple, Quick and Error-Free Layout
(Photo Courtesy of Metronome Systems Inc.)

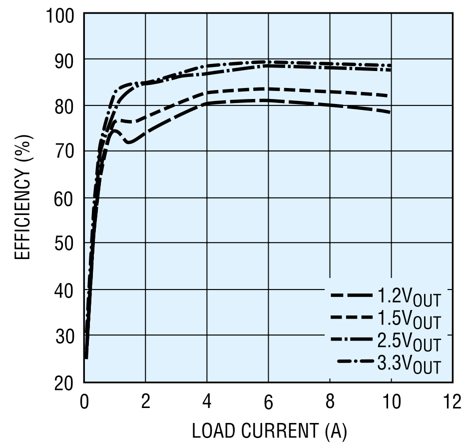


Figure 4. Efficiency vs Load Current wIth $12V_{IN}$

photos, under variety of conditions, is available at www.linear.com/micromodule.

High Input Voltage, Ultrafast Transient Response

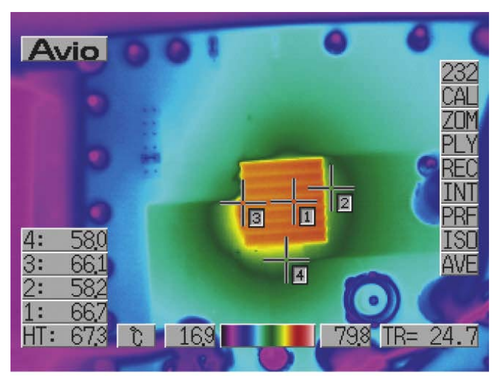
The LTM4600, unlike other DC/DC POL modules that have limited input range, can convert input supply voltages as high as 28V, without any input supply protection or additional external components. The output voltage is adjustable from 0.6V to 5V with ±1.5% accuracy.

A unique capability of the LTM4600 is its no-clock latency current mode architecture, allowing it to respond quickly to rapid load current changes (Figure 6). Where other modules must wait one full clock cycle before responding to a load change, the LTM4600's response is instantaneous, dramatically reducing required bulk load capacitance.

20A Load Current by Paralleling Two µModules

Two LTM4600 µModules can be easily paralleled to provide up to 20A of output current. The µModule features a current mode control scheme that ensures excellent current sharing among the devices. Sharing the load current among two µModules and balancing the power dissipation minimize the thermal stress and reduce requirements for heatsinking and airflow.

By interconnecting only three pins between two LTM4600s, a power supply can be easily scaled for higher output current. All the necessary circuitry for balanced and accurate current sharing is integrated. There are no requirements for external op amps or other supporting components. Refer to the LTM4600 data sheet for details and the schematic for a 20A at 2.5V output from a 4.5V to 20V input supply.



CONDITIONS: 25°C, NO AIR FLOW,
WAKEFIELD ENGINEERING PN# CIS20069,
15mm × 15mm × 9mm HEATSINK, NO $EXTV_{CC}$

Figure 5. Low Thermal Impedance Prevents Overheating by Efficiently Dissipating Heat Even at Full Output Power

Complete 10A Switchmode DC/DC Power Supply in an IC Form-Factor

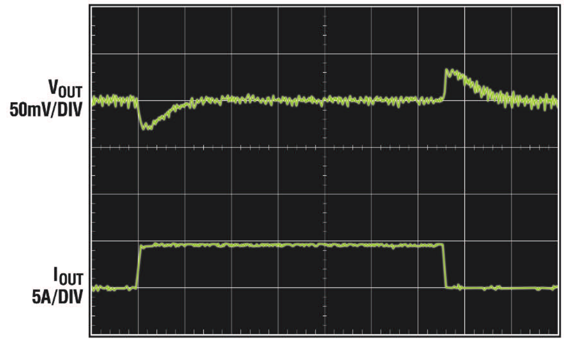


Figure 6. No-Clock Latency Current Mode Architecture for Ultrafast Transient

RoHS Compliant: Mounts with Both Pb-Based and Pb-Free Solder Pastes

The LTM4600 is RoHS compliant. However, unlike many Pb-free packages which include matte-tin lead finish, the LTM4600 is offered with gold-finish pads. Gold-finish pads allow the µModule to be used with either PbSn- or SnAgCu-based solder pastes for surface mount processing (Figure 7). This unique feature is especially attractive to companies planning to convert to Pb-free manufacturing but must qualify the LTM4600 immediately for surface mounting with Pb-based pastes.

Only 1.73 Grams

With its tiny and low profile size, the LTM4600 weighs only 1.73g. Therefore, this high voltage and high power supply requires no special surface mount tooling procedures. The µModules' light weight and small size is easily handled by the same pick-and-place machines as those used for FPGAs and microcontrollers. This compatibility streamlines the manufacturing of high density system boards such as AdvancedTCA or CompactPCI.

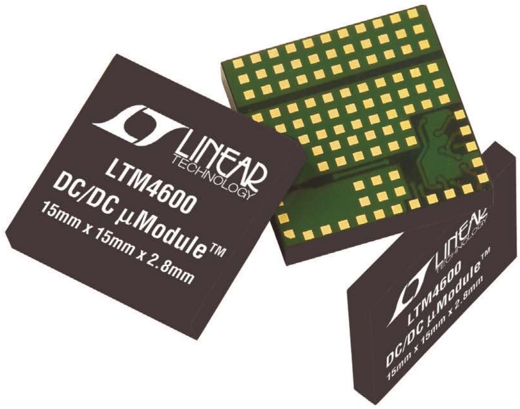


Figure 7. Gold-Finish Pads Allow the LTM4600 to Be Mounted with Pb-Based or Pb-Free Solder Pastes

BY GARY DROSSEL • SILICONSYSTEMS INC

Accurately judging endurance for solid-state storage

DETERMINING THE APPROPRIATE SOLID-STATE-STORAGE APPROACH FOR OEM APPLICATIONS CAN BE DIFFICULT, ESPECIALLY WHEN SUPPLIERS OFTEN RELY ON VARYING METHODS TO MEASURE THE PERFORMANCE OF THEIR PRODUCTS. IT IS NO WONDER THE SELECTION PROCESS IS DAUNTING.

Designers require a common measure for accurately evaluating storage options and their reliability. Endurance can provide such a measure, and understanding how to evaluate it correctly can help designers effectively select the right approach. "Endurance" refers to the number of write/erase cycles that a product can perform before it wears out. However, endurance is more than just a function of the storage media you are evaluating. The media and the associated controller technology combine to define a product's endurance. For example, magnetic media is an order of magnitude less reliable than NAND flash, yet the controller technology that rotating hard drives employ can compensate reasonably well for this deficiency.

Vendors specify write/erase-cycle endurance for solid-state storage in many ways. Some specify the endurance at the physical-block level, others specify it at the logical-block level, and still others specify it at the card or drive level. Because endurance also relates to data retention, you can calculate endurance at a higher level if the data-retention requirement is lower. For these reasons, it is often difficult to make an "apples-to-apples" comparison of write/erase endurance by solely relying on these numbers in a data sheet.

To most appropriately measure endurance, you must break specification data into three criteria: storage-media type, wear-leveling algorithms, and error-correction capabilities. Additional factors that affect endurance include the amount of spare sectors available and whether the storage device performs a write using a file system or direct logical-block addressing. Although these issues can contribute to the overall endurance calculation, their effects on the resulting number are much lower than those of the first three criteria.

STORAGE-MEDIA TYPE

The first of three critical steps in selecting the right solid-state-storage media is to compare media types, including both NOR and NAND flash. Current NOR-technology implementations generally find use only in cell-phone and other chip-on-board applications. For these applications, NOR provides execute-in-place, boot, and data-storage functions in one chip. The economies of scale and component densities of NAND make it a better approach than NOR for nonvolatile, solid-state-storage systems.

The two dominant NAND technologies are SLC (single-level cell), or binary, and MLC (multilevel cell). SLC technology stores one bit per cell, and MLC stores two bits. SLC NAND is generally specified at 100,000 write/erase cycles per block with 1 bit of ECC (error-correction code), whereas MLC is specified at 10,000 cycles with ECC. Although a data sheet for an MLC device may not specify the level of required ECC, MLC manufacturers recommend 4-bit ECC when using this technology. So, when using the same controller, a storage system using SLC has an endurance value roughly an order of magnitude higher than that of a similar MLC-based product.

WEAR-LEVELING ALGORITHMS

A wear-leveling algorithm allows storage media to have evenly distributed data writes and allows the controller in the storage media to remap logical-block addresses to different physical-block addresses in the solid-state memory array. The frequency of this remap, the algorithm to find the least worn area on which to write, and any data-swapping capabilities are generally proprietary intellectual property of the controller vendor. An integrated controller in the solid-state-storage system, which is independent of the host system, performs wear leveling. The host system performs its reads and writes only to logical-block addresses. So, as far as the host is concerned, the data never moves.

Three scenarios to consider when discussing wear leveling are no wear leveling, dynamic wear leveling, and static wear leveling. Flash cards for the retail consumer market and those for solid-state-storage systems for industrial applications differ greatly in endurance specs. A flash card that uses no wear leveling stops operating once the physical blocks wear out and all the spare blocks are exhausted, regardless of how much storage space remains unused. Early flash cards used no wear leveling and thus failed in write-intensive applications. For this reason, vendors do not recommend flash without wear leveling for use in enterprise-system OEM applications requiring industrial-grade, solid-state storage.

Dynamic wear leveling wears levels only over dynamic, or "free," areas. Systems using dynamic wear leveling do not touch static data. In a system using 75% of storage for static data, only 25% is available for wear leveling. So, you calculate the endurance of this approach as 25 times greater than a card with no wear leveling, but only one-fourth that of an approach that wear-levels over the entire storage space.

A static-wear-leveling algorithm evenly distributes data over an entire system and searches for the least used physical blocks. Once it finds them, it writes the data to those locations. If blocks are empty, the write occurs normally. If they contain static data, it moves that data to a more heavily used location before it moves the newly written data. You calculate the endurance of a storage system using static wear leveling to be 100 times better than an approach without wear leveling. A system with 75% of the storage containing static data is four times better than a card that implements dynamic wear leveling. Static wear leveling provides better endurance because it writes data to all blocks of the storage system.

ERROR-CORRECTION CAPABILITIES

Part of the solid-state memory-component specification relates to error correction, an equally important consideration for measuring endurance. For example, SLC NAND components perform 100,000 write/erase cycles with 1-bit ECC. It stands to reason that the specification would increase with a better error-correction algorithm. Most flash cards employ ECC algorithms with 2- to 4-bit correction, and a few industrial-grade, solid-state-storage systems employ as much as 6-bit correction. The terms "2-bit," "4-bit," and "6-bit" correction can be slightly confusing, because they refer to bytes in a 512-byte sector. For example, 6-bit correction defines the ability to correct as many as 6 bytes of data in a 512-byte sector. Because a byte equals 8 bits, a system with 6-bit ECC can correct 48 bits, as long as those bits stay within 6 bytes in the sector. The same definition holds true for 2- and 4-bit ECC.

The relationship between the number of bytes per sector that a controller can correct is not directly proportional to the overall endurance of a storage system, because the bit-error rate of NAND flash is not linear. Actually, 6-bit error correction should be much more than three times better than 2-bit ECC, because the probability of a 3-bit error is significantly greater than the probability of a 7-bit error.

THE ENDURANCE CALCULATOR

You can use the following equations to get an idea of how long a solid-state-storage system will last in an application. These calculations are valid only for products that use either dynamic or static wear leveling. You use solid-state-memory-component specifications for products that use no wear leveling. To calculate the expected life in years a product will last, use the following equation:

$$\text{YEARS} = \frac{(\alpha-\beta)\times\lambda\times(1-\varphi)}{(\omega\times\xi)\times k},$$

where α is the capacity in megabytes, β is the amount of static data in megabytes, λ is the block-level endurance specification, ϕ is the safety margin, ω is the file size in megabytes, ξ is the number of writes of file size ω per minute, and k is the number of minutes per year. For the α calculation, when converting from gigabytes to megabytes, megabytes equal the gigabytes times 1024. Note that you need to calculate β, the static data, only for cards that use a dynamic-wear-leveling algorithm. This value should be zero for static wear leveling.

When calculating λ, the block-level endurance, the point is to determine the true endurance of a product—not the length of time a vendor claims it will last. Rather than use the specification on the component vendor's data sheet, obtain block-level-endurance specifications directly from the storage provider and ensure that you have the endurance specification at the block level and not for the card or system. Many vendors specify endurance at the card level, so be careful to use the proper value for this variable. Base the user-defined ϕ, or safety margin, on the confidence of the data-transaction numbers that follow. For ω, the file size, when converting from megabytes to kilobytes, megabytes equal kilobytes divided by 1024. When calculating k, the number of minutes per year, the formula is: 60 minutes/hour×24 hours/day×365 days/year=525,600.

To calculate the number of data transactions, use the following equation:

$$\text{TRANSACTIONS} = \frac{(\alpha-\beta)\times\lambda\times(1-\varphi)}{\omega},$$

where all of the symbols carry the same meaning as they do in the expected-life calculation.

Designers will continue to face challenges in their selections as solid-state-storage manufacturers and flash-card providers vie for their attention. As part of their evaluation, designers will note differing requirements for industrial-OEM applications and for consumer applications, so it is important to distinguish between a flash-card supplier and a developer of solid-state storage.

Although it is valuable to evaluate solid-state-storage systems based on the type of media, it should never be your only consideration. The controller's ability to compensate for the media is an even more significant issue. Additionally, the use of wear leveling and ECC can dramatically affect the reliability and enhance the usable life of the solid-state-storage system in an application. Taking all of these parameters into consideration should help designers more easily wade through the selection process and ultimately select the best approach for their application. **EDN**

AUTHOR'S BIOGRAPHY

Gary Drossel is director of product marketing at SiliconSystems (Aliso Viejo, CA), which he joined in 2004. He is responsible for managing marketing and business development for the company's product line. A 15-year industry veteran, Drossel has also played a leading role in developing the company's marketing strategy, including product roll-outs and customer introductions. He received a bachelor's degree in electrical and computer engineering from the University of Wisconsin (Madison).

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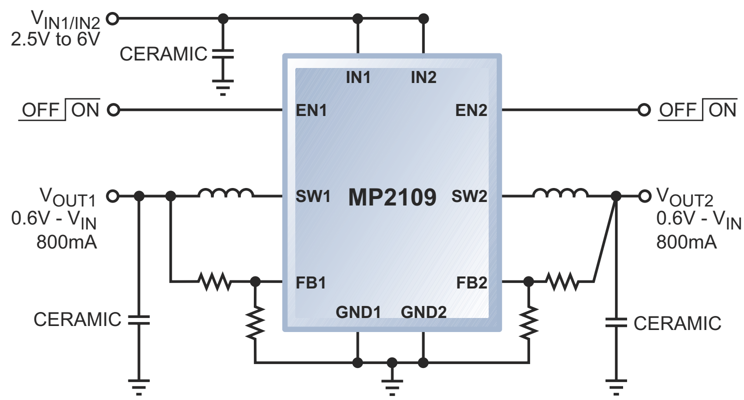

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Part	Frequency	V_{IN} (V)	I_{OUT} (A)	Package
Featured Synchronous Bucks				
MP2104	1.7MHz	2.5 - 6	0.6	TSOT23-5
MP2109*	1.0MHz	2.5 - 6	2x 0.8	QFN10 (3x3)
MP2106	800kHz	2.6 - 15	1.5	QFN10 (3x3)
MP2305	340kHz	4.75 - 23	2	SOIC8
MP1570	340kHz	4.75 - 23	3	SOIC8
Featured Non-Synchronous Bucks				
MP2361	1.4MHz	4.75 - 23	2	QFN10 (3x3)
MP2364*	1.4MHz	4.75 - 23	2x 1.5	TSSOP20
MP2354	380kHz	4.75 - 23	2	SOIC8
MP1593	385kHz	4.75 - 28	3	SOIC8

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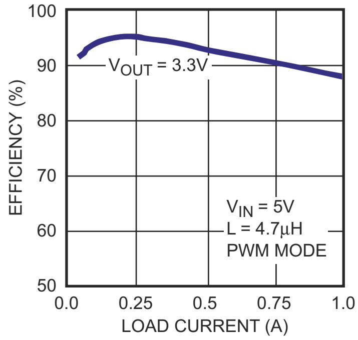

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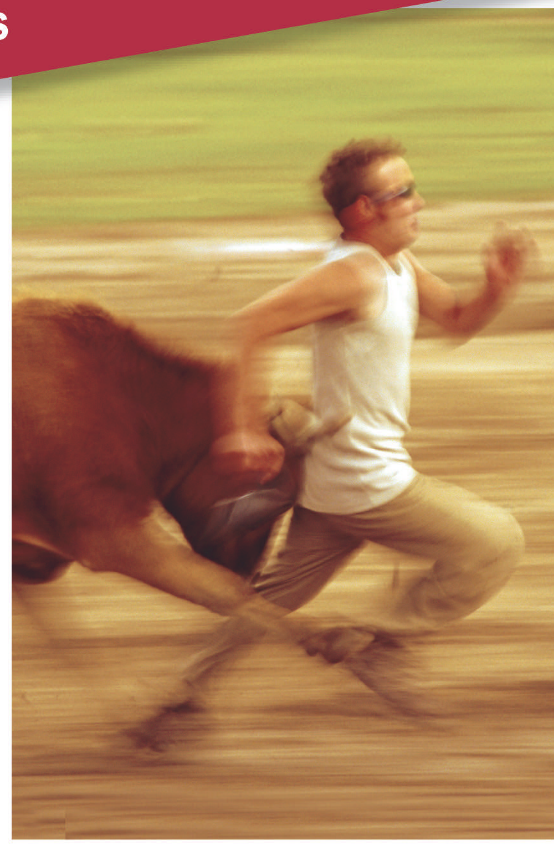

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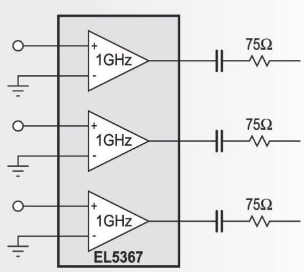

Part No.	BW (MHz)	SR (V/µs)	I_S (mA)	A_V (min) (V)	I_{OUT} (mA)	V_{OUT} (V)
EL5360	200	1700	0.75	1	70	±3.4
EL5362	500	2500	1.5	1	100	±3.6
EL5364	600	4200	3.5	1	140	±3.8
EL5367	1000	6000	8.5	1	160	±3.8

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- 1.4GHz bandwidth
- 6000V/µs slew rate
- Less than 9mA power consumption

Part No.	# of Amps	BW (MHz)	SR (V/µs)	I_S (mA)	A_V (min) (V)	I_{OUT} (mA)	V_{OUT} (V)	V_{OS} (max) (V)
EL5160/1	1	200	1700	0.75	1	70	±3.4	5
EL5162/3	1	500	4000	1.5	1	100	±3.6	5
EL5164/5	1	600	4700	3.5	1	140	±3.8	3.5
EL5166/7	1	1400	6000	8.5	1	160	±3.8	5
EL5260/1	2	200	2000	0.75	1	70	±3.4	5
EL5262/3	2	500	2500	1.5	1	100	±3.6	5
EL5462	4	500	2500	1.5	1	100	±3.6	5

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- Virtually unlimited slew rate
- 700MHz gain of 1 bandwidth
- Almost zero overshoot
- Low power consumption

Part No.	# of Amps	BW (MHz)	SR (V/µs)	V_N (nV/√Hz)	I_S (mA)	I_{OUT} (mA)	V_{OUT} (V)	V_{OS} (max) (V)
EL5100/1	1	300	2200	10	2.6	100	±3.4	5
EL5102/3	1	400	2200	6	5.2	150	±3.7	5
EL5104/5	1	700	4500	14	9.5	160	±3.8	5
EL5202/3	2	400	2200	6	5.2	150	±3.9	5
EL5204/5	2	700	3000	10	9.5	160	±3.8	10
EL5300	3	200	2200	10	2.5	100	±3.4	4
EL5302	3	400	2200	6	5.2	150	±3.7	5
EL5304	3	700	3000	10	9.5	160	±3.8	10

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Clear calls from the road

VOICE-INTERFACE TECHNOLOGY IMPROVES THE SAFETY AND CLARITY OF HANDS-FREE COMMUNICATION IN AUTOMOBILES.

Talking and driving—a dangerous combination, for sure, yet popular for a generation that wants to stay in touch with family and friends, no matter where they are or what they are doing. "Of all the accessories for cell phones, the ones people most want are headsets and other hands-free devices," says research analyst Linda Barrabee, who last year surveyed mobile-phone-buying habits for the Yankee Group. With the advent of a standard wireless interface in cellular phones (Bluetooth), the hands-free function in automotive telematics is set for explosive growth over the next several years.

Over the past decade, technological advances have contributed to improvements in voice quality and enhanced recognition rates for the hands-free cellular-phone function. Since the early days of using a plain microphone as the input device in the car cabin, industrial engineers have designed special housing for microphones, DSP engineers have developed voice-processing algorithms, and several companies have ventured into array microphones.

Despite these considerable developments, two perceptible needs still remain for users: land-line-quality conversations and higher voice-recognition rates, especially at highway speeds. Limitations in current technology allow microphones to pick up noise from all around the car cabin. Such environments require a new technology to give consumers what they want.

HANDS-FREE-MARKET BACKGROUND

Road safety continues to be a major concern for everyone, including government agencies, car manufacturers, and drivers themselves. Anything that draws the driver's attention away from driving can make the roads hazardous—whether it is reading the newspaper, eating a sandwich, or talking on the phone. As such, hands-free cell-phone functions that allow drivers to keep both hands on the wheel and both eyes on the road are becoming essential features in today's automobiles.

Worldwide, about 25 countries, including Australia, Italy, Israel, and Japan, have passed laws restricting drivers from using handheld cell phones. Three US states, including New York, have enacted similar laws, and at least 40 other states are now proposing such legislation, according to the National Conference of State Legislatures. Although consumers must comply with these laws, they also want to enjoy their conversations. Today, there is still a noticeable difference in voice quality between using a handheld phone and using a hands-free device. On the other hand, service providers such as On-Star continually look to improve customer satisfaction, especially for the automated voice-activated systems.

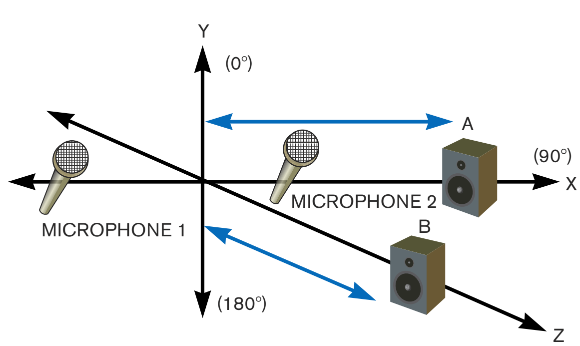


Figure 1 The traditional array microphone requires at least 30 mm between each microphone and can cancel noise only on a 2-D plane.

TECHNOLOGY TREND

Historically, hands-free-telematics functions have used a single microphone as the input interface. This microphone could be unidirectional or omnidirectional and strategically placed within the cabin—on the visor, steering wheel, or rearview mirror, for example. Although this setup served its purpose in picking up the talker's voice, it also picked up all of the surrounding noise and echo, which quickly became unbearable for the far-end user.

Industrial designers quickly realized that, by using special acoustically designed microphone housings, they could block out a certain level of noise while focusing the microphone pickup at a certain location. Although this arrangement helped to increase the SNR (signal-to-noise ratio), echo still remained a pestering concern.

A big step in making hands-free telematics a widely acceptable feature was the deployment of AEC (acoustic-echo-cancellation) and noise-suppression software. Running on either general DSP platforms or on dedicated IC chips, these algorithms can reduce acoustic echo by 45 dB and suppress stationary noise by 10 dB. AEC and noise-suppression signal processing have significantly improved the voice quality of hands-free conversations in the car cabin. However, for many of these software-DSP products, the user experience has still not reached the point at which everyday consumers could comfortably use the hands-free function. Users have given mixed reviews of several hands-free-car-kit models using software DSP on the mar-

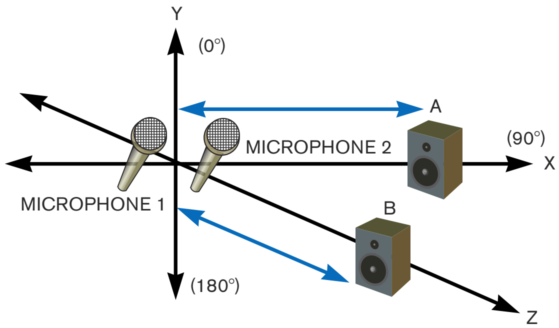


Figure 2 SAM beam-forming technology uses one unidirectional microphone and one omnidirectional microphone that you can place very close to each other (5 mm, center to center).

ket today, complaining about distorted sounds and robotic-sounding voices.

ARRAY AND SMALL-ARRAY MICROPHONES

The big leap in voice-interface technology is the array microphone. By arranging multiple microphones in an array, companies such as Fortemedia (www.fortemedia.com), AKG (www.akg.com), Knowles Acoustics (www.knowlesacoustics.com), and even Microsoft (www.microsoft.com) can further reduce surrounding noise, providing a more natural-sounding voice. Leveraging the information gathered by the multiple microphones about the voice and surrounding environment, an array microphone can process the signals in such a way that effectively forms a beam to pick up the wanted signal and cancels out noise outside the beam. Jaguar (www.jaguar.com) and Mercedes Benz (www.mercedes-benz.com) have deployed several hands-free car kits using array microphones in their XK models and E-Class cars, respectively, for example.

Although there are improvements in noise suppression, the traditional array microphone is still impractical and limited in two ways. First, it requires at least 30 mm between each microphone, putting placement and space constraints on the end technology. Second, it can cancel noise only on a 2-D plane, which makes it harder to pinpoint the talker and allows noise to leak into the beam. Diffused noise, engine noise, rattling of the dashboard, and general road noise coming from above and below the pie-shaped beam cause major problems for voice-recognition-related applications.

A new technology, SAM (small-array microphone), is the next step in the voice-interface market for noise-free communication. Designers can use SAM, placing the microphones only 5 mm apart (center to center), in practically any situation or application. SAM uses a fundamentally different algorithm from the traditional array microphone to process the voice, effectively forming a 3-D cone-shaped beam. As such, the system cancels out any noise outside the beam, whether above or below, without any leakage.

TRADITIONAL BEAM-FORMING

Traditional beam-forming uses the time delay between signals received at different microphones in the array. As such, the microphones are farther apart so that the information that each microphone receives is sufficiently different. The width of a broadside-array beam is based on the wavelength of the signal divided by the length of the aperture. So, at low frequencies at longer wavelength, the beam needs to be wider than that of higher frequencies at shorter wavelength.

Due to the need to process the difference in time delay and the need to capture frequencies of 300 Hz to 3.3 kHz, the traditional array microphones need to be at least 30 mm apart. This requirement brings about many limitations.

In **Figure 1**, the two microphones are facing 0°, meaning that the beam center is the y axis. Now, assume the signal source at Point A is playing at the same decibel level as the signal source at Point B. Also assume that Point A and Point B are the same distance away from the center of the array. In this case, the signal from Source A is suppressed, because the array microphone can obviously detect that Source A is outside the beam. (Time

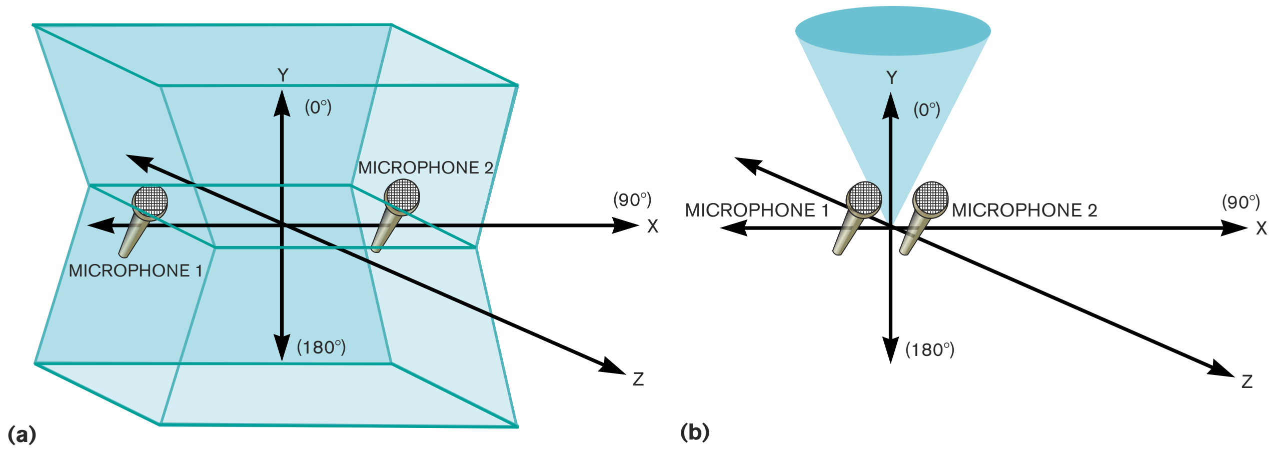


Figure 3 Offering many advantages over the traditional array microphone (a), the effective beam of a SAM is 3-D and cone-shaped (b).

Intersil Interface Products

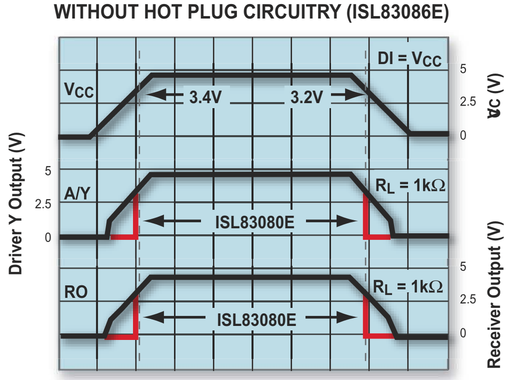
Intersil High Performance Analog

Want a More Dependable Bus?

Try a better Transceiver. Intersil's new ISL8308XE 5V Fractional (1/8) Unit Load, RS-485/RS-422 Transceivers incorporate "Hot Plug" functionality to keep your bus from crashing during power-up and power-down.

That's not all. These devices feature 15kV ESD Protection; "Full Fail-Safe" design to ensure a high Rx output if Rx inputs are floating, shorted, or terminated but undriven; and low bus currents to allow up to 256 transceivers on the network without violating the RS-485 network specification's 32 unit load maximum without using repeaters.

HOT PLUG PERFORMANCE (ISL83080E) vs DEVICE WITHOUT HOT PLUG CIRCUITRY (ISL83086E)



Key Features:

- True 1/8 Unit Load allows up to 256 devices on the bus
- Hot Plug circuitry to maintain three-state Tx and Rx outputs during power-up and power-down
- Full Fail-Safe (open, short, terminated and floating) receivers
- ±15kV HBM ESD Protection on RS-485 I/O pins and Class 3 ESD Protection on all pins
- Available in Pb-Free and small MSOP packages

Datasheet and more info available at **www.intersil.com/edn**

5V, High ESD, Fractional (1/8) Unit Load RS-485/RS-422 Key Specifications

Device	# of Tx/ # of Rx	Devices Allowed on Bus	Half/ Full Duplex	High ESD?	Hot Plug?	Data Rate (Mbps)	Slew Rate Limited?	Tx/Rx Enable?	ICC EN / DIS (µA)	SHDN ICC (µA)	VCC Range (+V)	Pkg.
ISL83080E	1 / 1	256	Full	Yes	Yes	0.115	Yes	Yes	530 / 530	0.07	4.5 to 5.5	14 Ld SOIC
ISL83082E	1 / 1	256	Half	Yes	Yes	0.115	Yes	Yes	560 / 530	0.07	4.5 to 5.5	8 Ld MSOP 8 Ld SOIC
ISL83083E	1 / 1	256	Full	Yes	Yes	0.5	Yes	Yes	530 / 530	0.07	4.5 to 5.5	14 Ld SOIC
ISL83085E	1 / 1	256	Half	Yes	Yes	0.5	Yes	Yes	560 / 530	0.07	4.5 to 5.5	8 Ld MSOP 8 Ld SOIC
ISL83086E	1 / 1	256	Full	Yes	No	10	No	Yes	530 / 530	0.07	4.5 to 5.5	14 Ld SOIC
ISL83088E	1 / 1	256	Half	Yes	No	10	No	Yes	560 / 530	0.07	4.5 to 5.5	8 Ld MSOP 8 Ld SOIC

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HIGH PERFORMANCE ANALOG

delay to Microphone 1 is much longer than time delay to Microphone 2.) However, the signal from Source B is not suppressed; to the traditional array microphone, Source B is effectively in the middle on the beam, because the difference in time delay is exactly the same to Microphone 1 as to Microphone 2. This limitation applies to every plane throughout the z axis, as well as directly behind the array (180°). Thus, the traditional array microphone can effectively suppress noise only in a 2-D manner. (In this example, the system cancels noise only on the xy plane.)

SAM-BEAM-FORMING

SAM-beam-forming technology is unlike traditional setups. It uses one unidirectional microphone and one omnidirectional microphone. Because you can place these two microphones only 5 mm away from each other center to center, the information coming to both microphones is highly correlated—virtually the same. Consequently, the beam-forming capability relies on the intelligence of Fortemedia's patented voice-processing algorithm to decipher this information.

Because you can place microphones of a SAM virtually right next to each other, the effective beam is a 3-D cone-shaped beam, which offers many advantages over the traditional array microphone. The setup in **Figure 2** is the same as in **Figure 1**, except the receiving device is a SAM instead of the traditional array microphone. To the SAM, the signals from Source A and Source B are exactly the same—in this case, both outside the beam. This situation applies throughout the y axis, forming a 3-D cone-shaped beam. The technique effectively suppresses noise above, below, and behind the beam. **Figure 3** compares the effective beam of a traditional array microphone with that of a SAM.

VALUE TO END USERS

We've come a long way since the early days of using just a plain microphone as the input device. Undoubtedly, we will continue to use the phone in the car. And, based on legislative developments around the world, we will need to do it using hands-free kits. So, what does this situation mean for users? With SAM technology, On-Star users, for example, will experience higher voice-recognition rates when using the automated systems; the systems will suppress engine noise, road noise, and the rattling of the dashboard. Users will also be able to barge in and interrupt the automated system when necessary. During a person-to-person conversation, the far-end user will never notice the noises and rattles from the car cabin. With the SAM, calls you make in the car will be just as clear as calls you make from your living room. EDN

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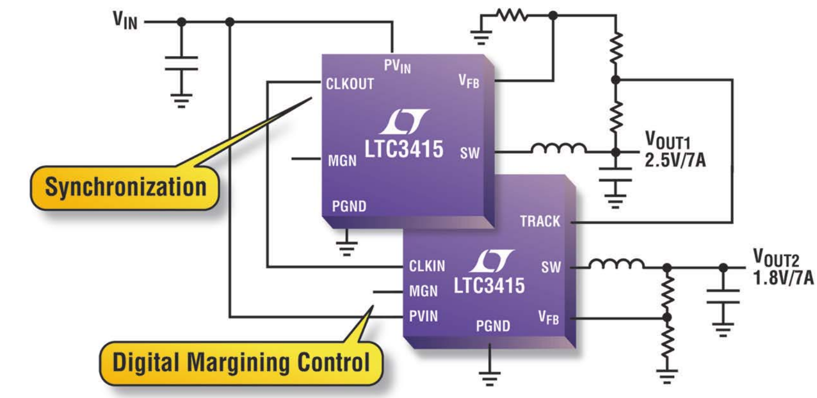
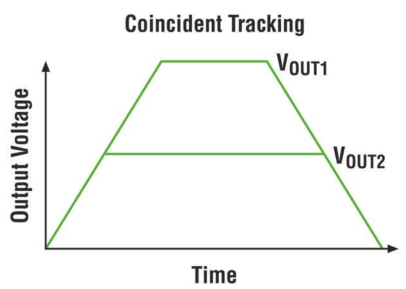
AUTHOR'S BIOGRAPHY

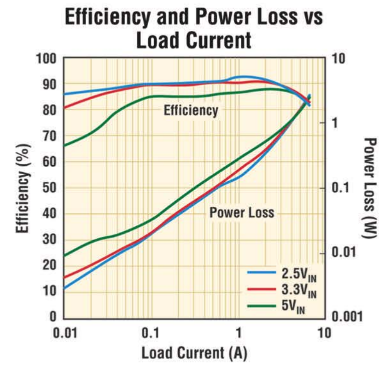
Samuel Yu is a product-marketing manager at Fortemedia. He received a bachelor's degree in electrical engineering and computer science from the University of California—Berkeley.

BIG POWER

Small Size







Trackable, Phase-Lockable, Current Sharing Monolithic DC/DC Converters

Obtaining a high current output in a compact circuit footprint is easy–thanks to Linear's growing family of high switching frequency, synchronous monolithic step-down DC/DC converters. Key features include current mode topologies for excellent line and load transient response, spread spectrum operation for low EMI, output currents up to 8A from a single package, high conversion efficiency to minimize thermal issues, input tracking for easy supply sequencing and the ability to stack multiple converters in parallel for accurate current sharing of up to 84A output current.

Selected Monolithic Converters

Part Number	V_{IN} Range (V)	I_{OUT} (A)	Freq. (MHz)	Package	Features
LTC®3412	2.625 to 5.5	2.5	4	TSSOP-16E/QFN	$V_{OUT(MIN)} = 0.8V$
LTC3413	2.25 to 5.5	±3	2	TSSOP-16E	For DDR/QDR
LTC3414	2.25 to 5.5	4	4	TSSOP-20E	$V_{OUT(MIN)} = 0.8V$
LTC3416	2.25 to 5.5	4	4	TSSOP-20E	Tracking Input
LTC3415	2.5 to 5.5	7	2	QFN	PolyPhase®, Stackable
LTC3418	2.25 to 5.5	8	4	QFN	Tracking Input

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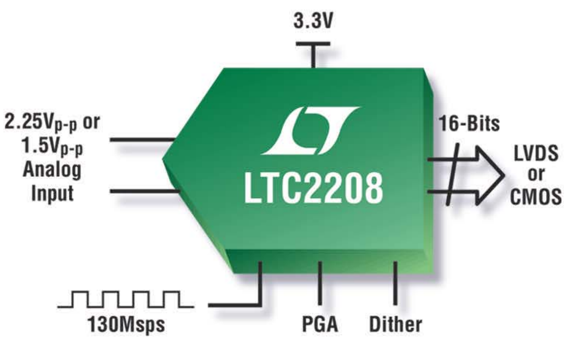
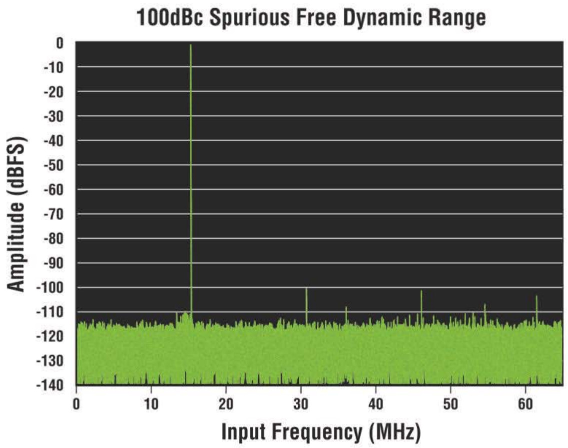
Literature: 1-800-4-LINEAR

Support: 408-432-1900

LINEAR TECHNOLOGY

16-Bit, 130Msps ADC





LTC2208 with Internal Dither Achieves 100dB SFDR from a Single 3.3V Supply

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Features

- 16-bits, 130Msps, 1250mW
- 78dB SNR, 100dB SFDR
- PGA Front End, 2.25V_{p-p} or 1.5V_{p-p} Input Ranges
- Internal Transparent Dither
- Digital Output Randomizer
- LVDS or CMOS Outputs
- Single 3.3V Supply
- Clock Duty Cycle Stabilizer
- 9mm x 9mm QFN Package

16-Bit ADC Family

Part No.	Speed	SNR	Power
LTC2208	130Msps	78dB	1250mW
LTC2207	105Msps	78dB	850mW
LTC2206	80Msps	78dB	650mW
LTC2205	65Msps	79dB	450mW
LTC2204	40Msps	79dB	350mW
LTC2203	25Msps	81dB	220mW
LTC2202	10Msps	81dB	150mW

Info & Online Store

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designideas

READERS SOLVE DESIGN PROBLEMS

Programmable analog circuits yield single-chip sinusoidal oscillators

Stefano Salvatori and Paolo Lorenzi, University of Rome, Rome, Italy

Programmable-logic devices provide a popular method of implementing complex functions in digital designs. Although manufacturers don't yet offer analog circuits whose complexity compares to VLSI digital circuits, field-programmable analog circuits are enjoying extensive use in signal-conditioning and filtering applications. Based on CMOS-operational-transconductance and switched-capacitor amplifiers, these devices offer a convenient approach to relatively complex design problems. Lattice Semiconductor's (www.latticesemi.com) ispPAC10 in-system-programmable analog circuit and its accompanying PAC Designer software offer a convenient method of circuit design and verification (**Reference 1**). This Design Idea presents two simple sinusoidal oscillators based on the ispPAC10.

Resistors within the ispPAC10 are fixed at a nominal 250 kΩ, and all capacitors are user-selectable from 1.07 to 61.59 pF. **Figure 1** shows an ispPAC10 with its internal blocks 1, 2, and 4 connected as a cascade of three first-order lowpass filters to form a classic phase-shift RC oscillator. Altering the capacitors' values produces oscillation frequencies over a range of 18 to 130 kHz. Each PAC block's gain is fixed at a factor of two to obtain a loop gain of −8, which Barkhausen's condition for oscillation requires (**Reference 2**). Configured from Block 3, a first-order lowpass filter reduces the THD (total harmonic distortion) on the oscillator's output. The values of capacitors in Block 3 are optimized for filtering performance and thus differ from those of the phase-shift stages.

The circuit in **Figure 2** describes a two-integrator loop that forms a classic quadrature-RC oscillator. The circuit's oscillation frequency spans 12 to 126 kHz and depends on the time con-

DIs Inside

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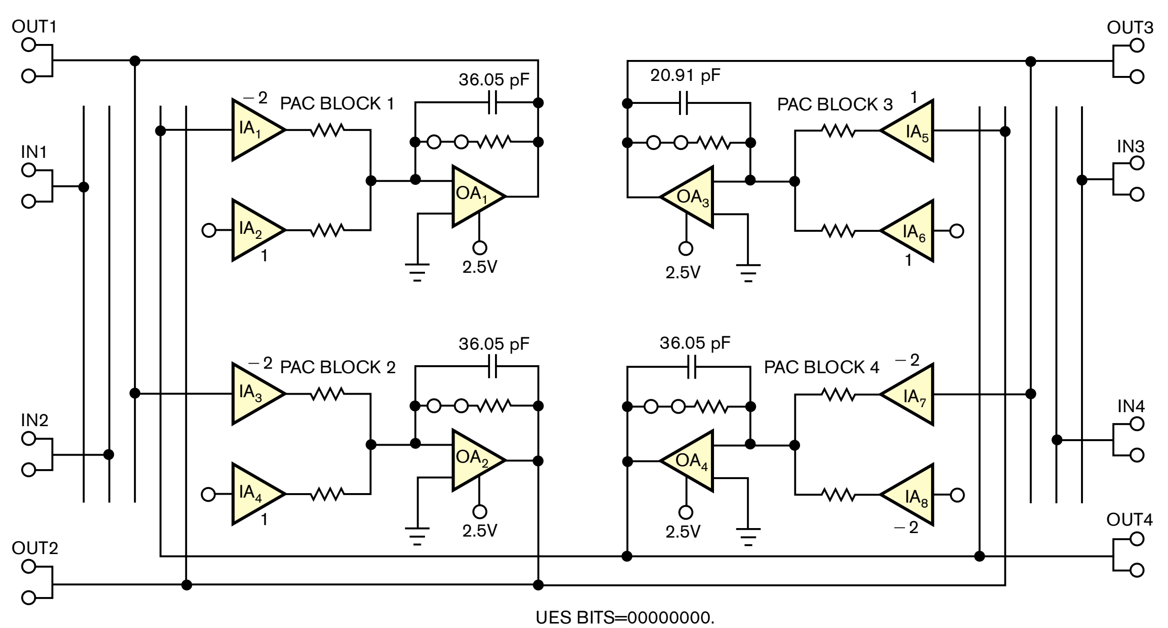


Figure 1 Based on a Lattice Semiconductor ispPAC10 programmable analog circuit, this phase-shift sine-wave oscillator and lowpass filter require no external components. The values are for a 30.4-kHz oscillator.

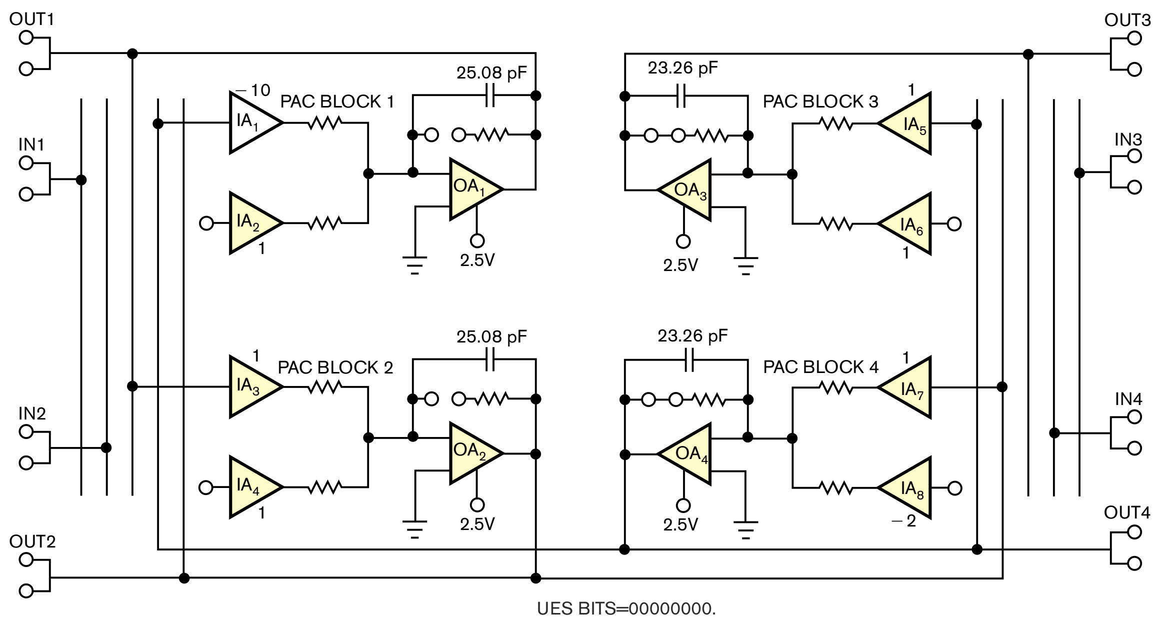


Figure 2 Cascaded dual integrators implement a quadrature sine-wave oscillator, with blocks 3 and 4 forming a low-pass filter. Again, the circuit design uses no external components. The values shown are for a 27.2-kHz oscillator.

stants of the integrators that blocks 1 and 2 form. In theory, each integrator's gain should have an absolute value of unity, but, in practice, ispPAC allows specification only of inverting integrators, and producing a stable sinusoidal signal requires a gain of at least −4 in Block 1. The circuit uses a gain of −10. Two additional blocks of the ispPAC10 device form a second-order lowpass filter that decreases the output's THD. In both oscillator circuits, you can alter the lowpass filters' gain so that the circuit's outputs deliver specific voltages, such as 1V p-p, at all frequencies.

Tables 1 and **2**, respectively, contain summaries of the phase-shift and quadrature oscillators' components and output characteristics. C_N refers to the value of the capacitor used in the

TABLE 1 PHASE-SHIFT OSCILLATOR

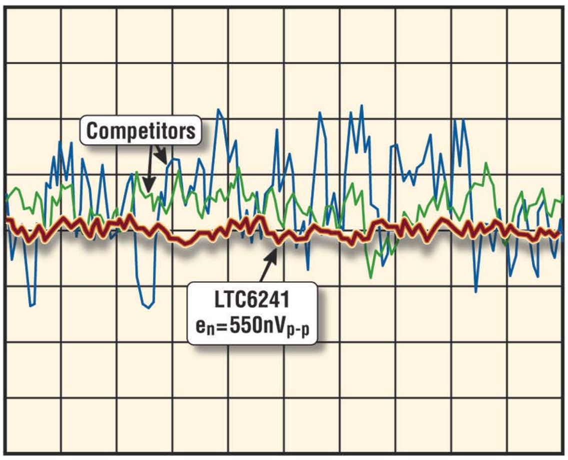
C_1 (pF)	C_2 (pF)	C_3 (pF)	C_4 (pF)	f_0 (kHz)	Δf (kHz) at −20 dB	THD (dB)
5.46	5.46	5.06	5.46	130.1	6	−25
6.92	6.92	5.92	6.92	115.4	6	−30
7.77	7.77	6.92	7.77	109.9	6	−30
9.19	9.19	6.92	9.19	97.8	2.5	−32
14.62	14.62	9.19	14.62	67.9	2.5	−39
20.91	20.91	12.78	20.91	50.1	2.5	−40
36.05	36.05	20.91	36.05	30.4	1.2	−40
61.59	61.59	35.25	61.59	17.7	0.6	−41

TABLE 2 QUADRATURE OSCILLATOR

C_1 (pF)	C_2 (pF)	C_3 (pF)	C_4 (pF)	f_0 (kHz)	Δf (kHz) at −20 dB	THD (dB)
1.07	1.07	5.06	5.06	125.9	6	−27
3.56	3.56	5.92	5.92	105.1	6	−25
5.92	5.92	7.77	7.77	80.4	2.5	−30
7.77	7.77	9.62	9.62	66.3	2.5	−34
14.22	14.22	15.45	15.45	41.7	2.5	−40
25.08	25.08	23.26	23.26	27.2	1.2	−40
40.08	40.08	26.29	26.29	18.6	1.2	−42
50.01	50.01	35.25	35.25	15	0.6	−42
61.59	61.59	40.98	40.98	12.3	0.6	−41

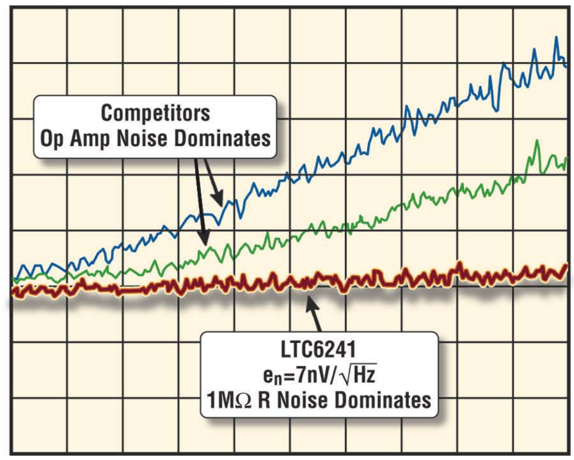
Low Noise CMOS

Low Frequency Noise

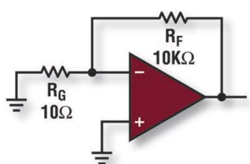


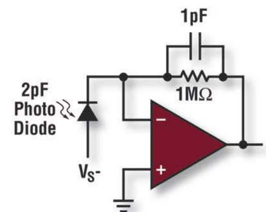
0.1Hz to 10Hz Input Referred Noise

High Frequency Noise



1kHz to 100kHz Noise Voltage Density





1pA, 125µV CMOS Amplifier Shatters the Noise Barrier

The LTC®6241 minimizes a fundamental error source, voltage noise, inherent in conventional CMOS amplifier designs. For the first time, designers of high precision systems can obtain superb DC precision with unprecedented low noise, with a high input impedance CMOS op amp. Featuring exceptionally low noise over a wide frequency range, the LTC6241 allows maximum signal resolution in demanding applications.

Features

- 0.1Hz to 10Hz Noise: 550nV$_{P-P}$
- 1pA Input Bias Current
- 125µV Max. Offset Voltage
- 2.5µV/°C Max. Offset Drift
- 124dB Voltage Gain
- 18MHz Gain Bandwidth Product
- 3pF Input Capacitance
- Rail-to-Rail Output
- 2.8V to 11V Supply Operation
- 3mm x 3mm DFN & SO-8 Packages
- LTC6241 (Dual): $1.25 each in 1k Qty.

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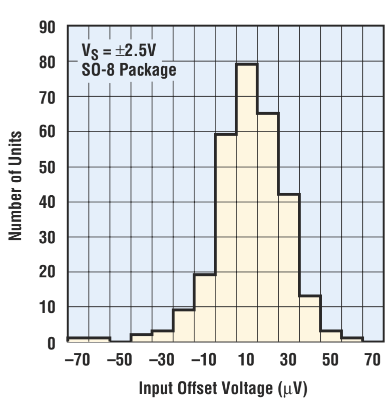

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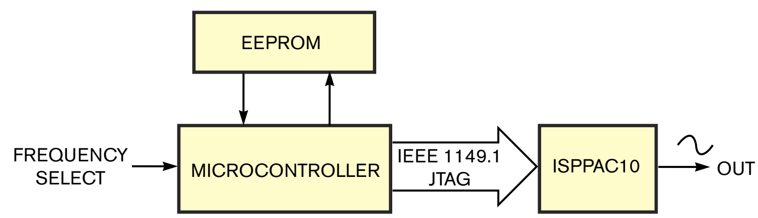

Figure 3 Either ispPAC10 circuit's implementation can serve as a foundation for a programmable oscillator by adding a microcontroller and nonvolatile storage.

nth PAC block for oscillation at frequency f_0. The design uses a Tektronix TDS1002 digital oscilloscope's FFT function to measure THD and the spectral line width of each output frequency at a level of −20 dB with respect to the central frequency, f_0.

Figure 3 illustrates the application of a microcontroller to dynamically reconfigure an ispPAC-based oscillator for specific frequencies. The nonvolatile memory stores frequency-specific capacitance and gain values for each of the ispPAC10's circuit blocks. Data transfers occur using the IEEE 1149.1 JTAG-standard protocol through the ispPAC10's serial test-access-port interface. EDN

REFERENCES

1. PAC Designer software, www.latticesemi.com.
2. http://jlnlabs.imars.com/spgen/barkhausen.htm.

Enhanced, three-phase VCO features ground-referenced outputs

Harry Bissell Jr, Welding Technology Corp, Farmington Hills, MI

Three-phase VCOs (voltage-controlled oscillators) see service in many applications, including power inverters and in electronic-music synthesis as control and modulation sources. A previous Design Idea describes a basis for a simple, three-phase VCO (**Reference 1**). However, adding a few components enhances the circuit's performance. The original circuit delivers an output of only 600 mV p-p and cannot tolerate substantial loading, especially at low operating frequencies at which the circuit draws the least operating current. Providing ac coupling for the output signals doesn't work well at low frequencies and worsens the loading problem. Finally, the circuit's dc operating point varies with frequency.

The circuit in **Figure 1** elegantly overcomes these limitations. The original circuit uses three of six of a CD4069UB hex inverter's subcircuits. One of the spares, IC_{1A}, senses the complete circuit's dc operating point. Resistor R_2 provides linear feedback around IC_{1A}, forcing the input voltage at Pin 9 to equal the output transition threshold voltage over a range of operating currents. In other words, the voltage is proportional to the average dc value of the sinusoidal output waveforms.

A voltage follower, IC_{2A}, buffers the averaged voltage at IC_{1A}'s Pin 8. The remaining sections of IC_2 buffer the oscillator's three outputs, equalizing the loading on the oscillator and providing low-impedance drive to three differential amplifiers: IC_{3A}, IC_{3B}, and IC_{3C}. The differential stages subtract the dc offset voltage from IC_{2A} from the buffered three-phase outputs. You can alter the voltage gain of the three differential amplifiers from its nominal factor of five to suit other applications.

Zener diode D_1 limits the voltage to 10V at IC_1's Pin 14. At low frequencies and currents, the oscillator's dc operating point can easily exceed the linear range of IC_2's inputs. You can use rail-to-rail-capable operational amplifiers instead of LM324-family devices. Note that the inputs of IC_1's remaining unused inverters connect to IC_1's Pin 7 and not to circuit ground per normal practice.

Adding an exponential current source eases the task of adjusting the circuit over a wide frequency range. Transistors Q_1 and Q_2 and their associated components form a simple exponential voltage-to-current converter. For best results, the base-emitter voltages of Q_1 and Q_2 should match at the circuit's nominal operating current—100 µA—and you should thermally couple both transistors. If your application requires precise thermal tracking, replace R_6 with a 2-kΩ temperature-compensating resistor with a coefficient of 3500 ppm/°C, such as a Tel Labs Q81, which is available from such companies as Precision Resistor (www.precisionresistor.com). Place this resistor in thermal contact with Q_1 and Q_2. Temperature-compensating resistors are also available from Micro-Ohm (www.micro-ohm.com), Vishay (www.vishay.com), Ultronix (www.ultronix.com), and KRL Bantry (www.krlbantry.com).

Using the component values in **Figure 1**, the circuit's operating frequency spans 0.1 to 26 Hz. Adding the components in this Design Idea reduces the circuit's dc operating-point shift from 5.5V to less than 25 mV over the frequency range. Most of the frequency

(continued on pg 84)

LINEAR TECHNOLOGY

DESIGN NOTES

Fast, High Efficiency, Standalone NiMH/NiCd Battery Charging

Design Note 380

Fran Hoffart

Introduction

Although recent popular attention is focused on Lithium Ion batteries, one must not forget that other battery chemistries, such as Nickel Cadmium (NiCd) and Nickel Metal Hydride (NiMH) have advantages in rechargeable power systems. Nickel-based batteries are robust, capable of high discharge rates, have good cycle life, do not require special protection circuitry and are less expensive than Li-Ion. Among the two, NiMH batteries are rapidly replacing NiCd because of their higher capacity (40% to 50% more) and the environmental concerns of the toxic cadmium contained in NiCd batteries.

The LTC®4010 and LTC4011 are NiCd/NiMH battery chargers that simplify Nickel-based battery charger design and include power control and charge termination for fast charging up to 16 series-connected cells using a synchronous buck topology. The LTC4011 provides a full feature set in a 20-lead TSSOP while the LTC4010 comes in a 16-lead TSSOP. The LTC4010 removes the PowerPath™ control output, top-off charge indicator, DC power sense input and provides limited thermistor options.

NiCd/NiMH Battery Charging Basics

Batteries come in many sizes and capacity ratings. When specifying charge current, it is commonly related to a battery's capacity, or simply "C". The letter "C" is a term used to indicate the manufacturers' stated battery discharge capacity which is measured in milliamp-hours (mAh). This capacity rating becomes important when fast charging because it determines the required charge current for proper charge termination.

There are several commonly used methods for charging Nickel batteries. They are all related to the length of the charge cycle which determines the recommended charge current. A slow charge (or low rate charge) consists of a relatively low charge current, typically 0.1C, applied for approximately 14 hours set by a timer. A quick charge applies a constant current of approximately 0.3C to the battery while a fast charge applies a constant current of 1C or higher. Both quick and fast charge cycles require that the charge current terminate when the battery becomes fully charged.

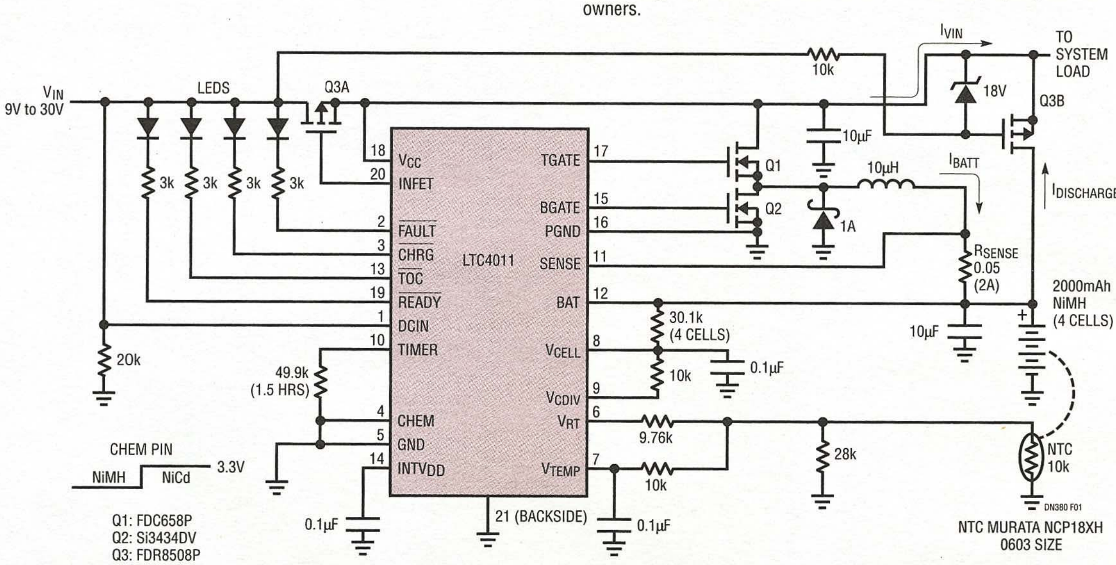

Figure 1. Full Featured Standalone 2A, 4-Cell NiMH Fast Charger with PowerPath Control

During a fast charge cycle, a constant current is applied to the battery while allowing the battery voltage to rise to the level required (within limits) to force this current. As the battery accepts charge, the battery voltage and temperature slowly rise. As the battery approaches full charge, the voltage rises faster, reaches a peak, then begins to drop ($-\Delta V$); at the same time, the battery temperature begins to quickly rise ($\Delta T/\Delta t$). Most fast or quick charge termination methods use one or both of these conditions to end the charge cycle.

Complete 4-Cell NiMH Battery Charger

Figure 1 shows a fast, 2A charger featuring the high efficiency LTC4011 550kHz synchronous buck converter. The LTC4011 simplifies charger design by integrating all of the features needed to charge Ni-based batteries, including constant current control circuitry, charge termination, automatic trickle and top off charge, automatic recharge, programmable timer, PowerPath control and multiple status outputs. Such a high level of integration lowers the component count, enabling a complete charger to occupy less than $4cm^2$ of board area.

Initial battery qualification verifies that sufficient input voltage is present for charging and that the battery voltage and battery temperature are within an acceptable range before charging at full current. For deeply discharged batteries, a low current trickle charge is applied to raise the battery voltage to an appropriate level before applying full charge current. When qualification is complete, the full programmed constant-current begins.

Standalone Charge Termination

The charge termination methods used by the LTC4010 and LTC4011 utilize battery voltage and battery temperature changes to reliably indicate when full charge is reached as a function of the charge current selected. The charge current must be sufficiently high (between 0.5C and 2C) for the battery to exhibit the voltage and temperature profile required for proper charge termination. Figure 2 shows a typical fast-charge profile displaying charge current, battery temperature and per cell voltage. This profile indicates that the charge cycle terminated due to the rate of temperature rise or $\Delta T/\Delta t$.

The $-\Delta V$ charge termination algorithm begins shortly after the full charge current starts flowing. A fixed delay time prevents false termination due to battery voltage fluctuations from batteries that are deeply discharged or haven't been charged recently. For batteries that are near full charge, the $-\Delta V$ termination sequence begins immediately to prevent overcharging.

During the charge cycle, both the $-\Delta V$ and $\Delta T/\Delta t$ termination methods are active. For NiMH batteries, the $-\Delta V$ termination requires that the single cell battery voltage drop 10mV from the peak voltage or the rate-of-temperature rise ($\Delta T/\Delta t$) be greater than 1°C/minute. The measurements are taken every 30 seconds and the results must be consistent for four measurements for termination to take place. Typically the $\Delta T/\Delta t$ termination method occurs earlier in the charge cycle. If this occurs, the LTC4010/4011 adds a top-off charge at a reduced charge current for 1/3 of the programmed time. Top-off only occurs when charging NiMH batteries.

After the charge cycle has ended, the charger continues monitoring the battery voltage. If the voltage drops below a fixed threshold level, due to an external load on the battery or self-discharge, a new charge cycle begins with the charge termination algorithms immediately enabled.

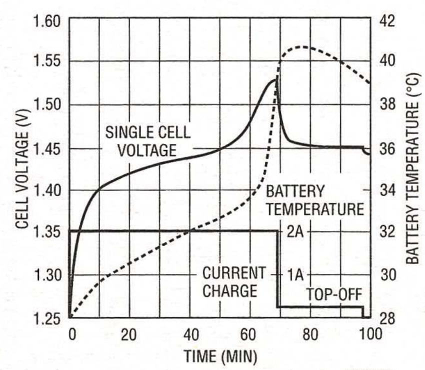

Figure 2. Typical NiMH Fast Charge Profile

Conclusion

The LTC4010 and LTC4011 provide complete standalone solutions for reliable, robust and safe fast charging of NiCd and NiMH batteries. Proper charging is critical to not only obtain maximum battery capacity but to also avoid high temperatures, overcharge and other conditions which adversely affect battery life.

Data Sheet Download

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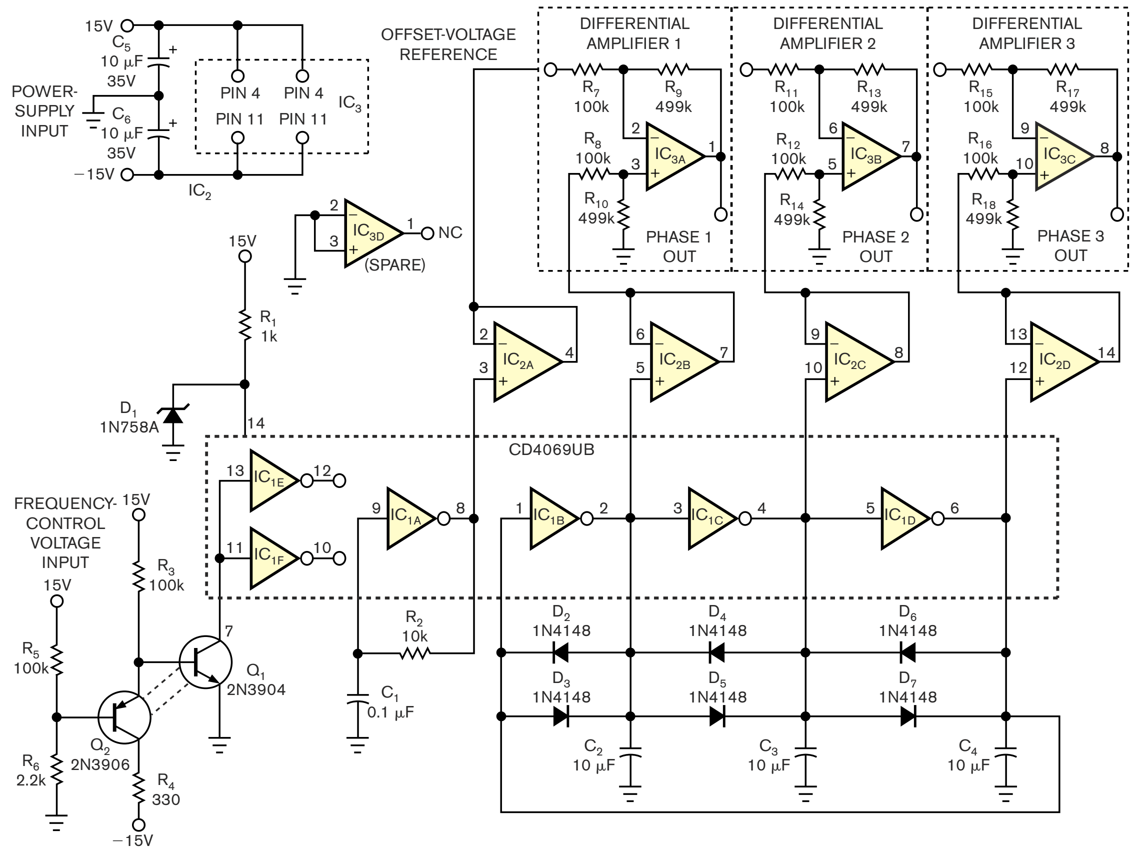
error occurs at the low end of the frequency range, at which it's the least objectionable.EDN

REFERENCE

1. Dutcher, Al, "Inverters form three-phase VCO," *EDN*, Aug 2, 2001, pg 102, www.edn.com/article/CA149120.



NOTES:
PLACE Q_1 AND Q_2 IN THERMAL CONTACT.
FOR BEST STABILITY, USE NONPOLARIZED CAPACITORS FOR C_2, C_3, AND C_4.
DOTTED LINES BETWEEN Q_1 AND Q_2 INDICATE THERMAL CONTACT.

Figure 1 Adding differential and buffer amplifiers and an exponential voltage-to-current converter enhances the performance of a low-frequency, three-phase voltage-controlled oscillator.

Improved current monitor delivers proportional-voltage output

Susanne Nell, Breitenfurt, Austria

This Design Idea expands the capabilities of a previously published one (**Reference 1**). The original version featured a current transformer whose secondary winding formed part of an oscillator's tank circuit. Under normal conditions, direct current flowing through the current transformer's single-turn primary winding kept the circuit from oscillating until primary current flow ceased. Although the circuit acted as a power-interruption detector, when you add a few components, the operating principle lends itself to measurement applications. This revised circuit delivers an accurate linear-voltage output that's proportional to direct current flow through current-sense transformer T_1's primary winding (**Figure 1**). In addition, the circuit also offers possibilities as an ac current sensor.

To achieve improved performance, the design retains the original oscillat-

ing-circuit concept and adds a PLL circuit and one additional winding to the current transformer whose secondary forms an LC oscillator's resonant circuit. Integrating a 74HC4046, IC_1, the PLL measures the frequency of an LC oscillator comprising Q_1 and its associated components and compares it with a fixed-frequency internal VCO (voltage-controlled oscillator). The PLL's phase-comparator output drives a current source comprising Q_2 and Q_3, which in turn feeds current to an additional winding on the current-sense transformer's core.

Sources of T_1's ferrite core include Epcos (www.epcos.com), which offers the B642-90L 632×87-toroid 20×10×7 material N87; Pramet (wwwpramet.com), which offers Fonox Type T20 material H60; Vacuumschmelze (www.vacuumschmelze.com), with the VAC T60006L2020-W409-52; and other manufacturers. Depending on the ferrite material you use, the circuit will operate to some degree with virtually any ferrite toroidal core. (It is difficult to simulate this circuit using PSpice or other simulators; for accurate results, you need a complex model that accurately portrays the core's nonlinear behavior at various current levels.)

The added winding induces magnetic flux in the core, decreasing its permeability and inductance and raising the LC oscillator's frequency. When the oscillator's frequency matches the VCO (reference) frequency, the circuit reaches an equilibrium state. An increasing or decreasing current through the compensation coil balances any additional magnetic flux that dc current flowing through the measurement coil produces.

Within the PLL's frequency-tracking range, the current waveform through the compensation coil has the same shape as fluctuations of the measured current. The turns ratio of 1-to-250, which also represents the ratio of currents in transformer T_1, establishes a secondary current of 10 mA for a primary current of 2.5A. If the PLL circuit's gain is sufficient and the ferrite core's region of operation avoids saturation, the circuit's closed-loop configuration maintains the core's magnetic flux at a constant value and thus minimizes the effects of core-material nonlinearities.

Measuring the voltage difference across resistor R_5 shows that the circuit's output voltage is linearly proportional to the compensation current, and R_5's resistance scales the voltage output. For 100Ω at R_5, a 1V output corresponds to a primary-side current of 2.5A. With zero current flowing in the single-turn primary winding, calibrate the circuit's range by adjusting potentiometer R_{11} to a set operating point. A voltage drop of 2V across R_5 sets a measurement range of +5 to −5A. To accommodate other measurement ranges, you can alter T_1's turns ratio or vary the compensation current by using different values for R_5 and R_{11}. Use a well-regulated power supply to provide power for the circuit. You may be able to replace the 74HC4046 with a software PLL-emulation routine that uses a microcontroller's spare processing resources. EDN

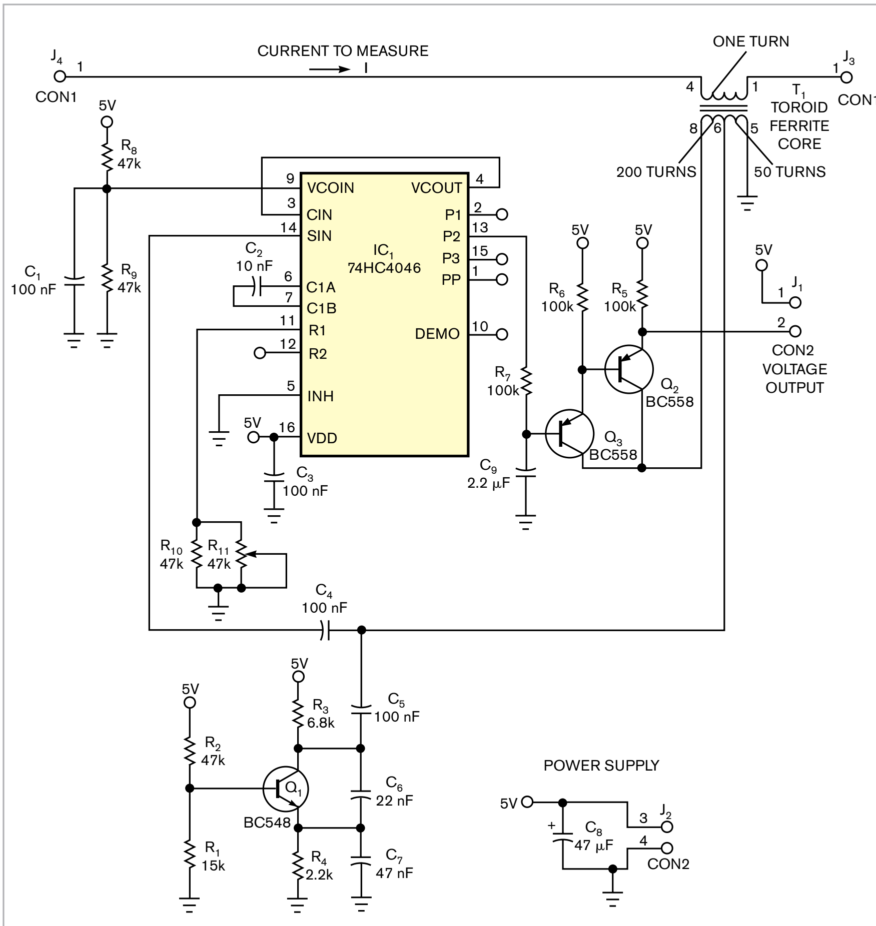
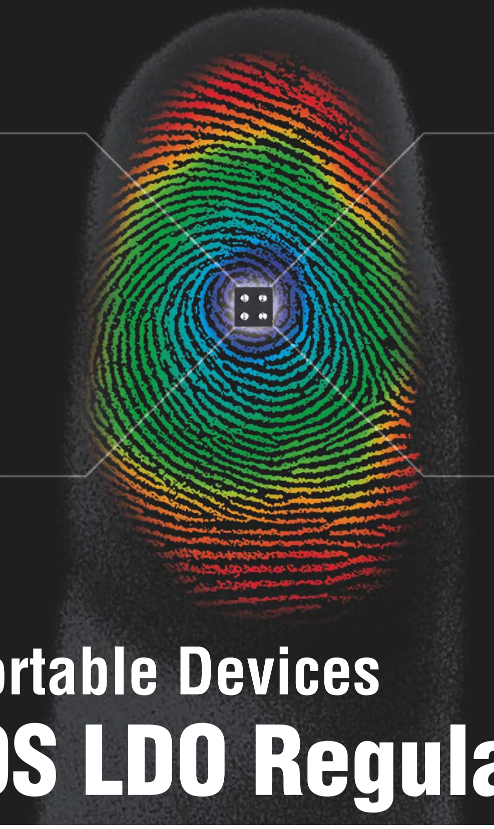


Figure 1 This current sensor uses a variable-frequency oscillator, Q_1, and a PLL, IC_1, to measure current in an isolated circuit.

REFERENCE

1. Ackerley, Kevin, "Impedance transformer flags failed fuse," *EDN*, Dec 17, 2004, pg 67, www.edn.com/article/CA486572.



Ultra-compact CSP package

0.1V LDO voltage

Compatible with ceramic capacitors

High-ripple rejection 63dB

Miniaturizing Portable Devices

ROHM CMOS LDO Regulators

Standard CMOS LDO Regulators

- Bi-CMOS process results in low current consumption 40μA ensuring suitability with portable equipment.
- 70dB ripple rejection rate due to built-in phase compensation circuit.

Part number	Output voltage (V)	Output voltage accuracy (%) (mV)	Output current (mA)	Input voltage (V)	Ripple rejection (dB)	Bias current (μA)	I/O voltage difference Io=100mA (mV)	Load regulation Io=1 to 100mA (mV)	Input capacitor (μF)	Output capacitor (μF)
BH□□FB1WG	2.5, 2.8, 2.9, 3.0, 3.1, 3.3	±1% (Vo=2.5 to 3.3V)	150	2.5 to 5.5	70	40	250	10	0.1	2.2
BH□□FB1WHFV										
BH□□LB1WG	1.5, 1.8	±25mV (Vo=1.5,1.8,1.85V)					—			1
BH□□LB1WHFV	1.5, 1.8, 1.85									

Large Current CMOS LDO Regulators

- Stable load regulation as low as 6mV.
- Ultra-low dropout voltage: 60mV.

Part number	Output voltage (V)	Output voltage accuracy (%) (mV)	Output current (mA)	Input voltage (V)	Ripple rejection (dB)	Bias current (μA)	I/O voltage difference Io=100mA (mV)	Load regulation Io=1 to 100mA (mV)	Input capacitor (μF)	Output capacitor (μF)
BH□□MA3WHFV	1.5, 1.8, 2.5, 2.8, 2.9, 3.0, 3.1, 3.3	±1% (Vo=2.5 to 3.3V) ±25mV (Vo=1.5,1.8V)	300	2.5 to 5.5	60	65	60	6	1	1

Ultra-compact CMOS LDO Regulators Suitable for High-density Mounting

- Highly reliable ultra-compact package.
- Ultra-compact CSP (Chip Size Package) for high power capability.

Part number	Output voltage (V)	Output voltage accuracy (%) (mV)	Output current (mA)	Input voltage (V)	Ripple rejection (dB)	Bias current (μA)	I/O voltage difference Io=100mA (mV)	Load regulation Io=1 to 100mA (mV)	Input capacitor (μF)	Output capacitor (μF)
BH□□RB1WGUT	1.5, 1.8, 2.5, 2.8, 2.9, 3.0, 3.1, 3.3	±1% (Vo=2.5 to 3.3V) ±25mV (Vo=1.5,1.8V)	150	2.5 to 5.5	63	34	100	2	1	1

High-ripple Rejection CMOS LDO Regulators for High-frequency Circuits

- High-ripple rejection rate of 80dB due to proprietary phase compensation circuitry.
- Stable load regulation: 6mV.

Part number	Output voltage (V)	Output voltage accuracy (%) (mV)	Output current (mA)	Input voltage (V)	Ripple rejection (dB)	Bias current (μA)	I/O voltage difference Io=100mA (mV)	Load regulation Io=1 to 100mA (mV)	Input capacitor (μF)	Output capacitor (μF)
BH□□NB1WHFV	2.5, 2.8, 2.85, 2.9, 3.0, 3.1, 3.3	±1% (Vo=2.5 to 3.3V)	150	2.5 to 5.5	80	60	250	6	0.1	2.2

CMOS LDO Regulators with Auto Power Saving Function

- Built-in auto power saving function limits standby current consumption.
- Output discharge function ensures a stable startup sequence.

Part number	Output voltage (V)	Output voltage accuracy (%) (mV)	Output current (mA)	Input voltage (V)	Ripple rejection (dB)	Bias current (μA)	I/O voltage difference Io=100mA (mV)	Load regulation Io=1 to 100mA (mV)	Input capacitor (μF)	Output capacitor (μF)
BH□□PB1WHFV	1.2, 1.5, 1.8, 2.5, 2.8, 2.9, 3.0, 3.1, 3.3	±1% (Vo=2.5 to 3.3V) ±25mV (Vo=1.2,1.5,1.8V)	150	1.7 to 5.5	60	2 (PowerSave) 20 (High-speed)	250	10	0.47	0.47

productroundup

OPTOELECTRONICS/DISPLAYS

Low-noise charge pump/linear regulator targets wireless-handset applications

Functioning as a charge pump and a linear regulator, the low-noise CM4072 LED driver runs at 250 kHz for powering white LEDs to backlight TFT (thin-film-transistor) LCDs in wireless devices. By integrating the charge pump and linear regulator into one chip, the charge-pump circuitry boosts the input voltage and sends it to the linear regulator to provide a constant 5V output and a 200 mA-output current. For brightness control of the white LEDs, the baseband processor sends a PWM signal to the enable pin. The device supports white LEDs at 25 mA each to backlight higher resolution QVGA TFT LCDs. The device also suits camera phones using a high-brightness camera-flash LED. It can drive three white LEDs at 65-mA maximum current or one high-brightness camera-flash LED at 200 mA. Available in a 3×3-mm, lead TDFN-10 package, the CM4072 costs 69 cents (1000).

California Micro Devices, www.calmicro.com

Multipurpose LED driver comes in small package

Suiting high-brightness LEDs in torch- or flash-system applications for cameras and portable electronic devices, the NCP5603 white-LED driver uses a charge-pump structure for power conversion. The device uses two external ceramic capacitors, eliminating the need for an inductor for power conversion. Due to 1, 1.5, and 2× automatic operating modes, the driver operates at 90% efficiency, targeting high-current LEDs in low-cost, low-power applications demanding extended battery life. The device provides a 350-mA output-current pulse, allowing it to drive a 1W, high-brightness power LED. Requiring no external inductor for energy storage, the driver also functions as a small boost dc/dc converter, supplying a constant voltage of 4.5 or 5V, aimed at biasing audio amplifiers in cell phones, MP3 players, and digital cameras. Available in a lead-free 3×3×9-mm DFN-10, the NCP5603 costs 70 cents (1000).

On Semiconductor, www.onsemi.com

Cell-phone-camera LED driver has low noise and high efficiency

The 850-kHz, 1×/1.5×/2× LTC-3217 multimode charge pump drives multiple high-current LEDs in cellular-phone-camera applications. Using constant-frequency operation for low noise, the device can drive four LED current sources at 600-mA total output current. Two logic-input pins select shutdown mode and current-output levels. A 2.9 to 4.5V voltage range targets single-cell lithium-ion inputs, providing a 92% efficiency for maximized battery runtime. Available in a 3×3-mm QFN-16, the charge pump requires four small capacitors and two resistors, creating a 20×20×0.75-mm footprint. Based on input-voltage and LED-forward-voltage conditions, the pump automatically optimizes efficiencies, powering up in 1× mode and switching to 1.5× boost mode when any enabled LED current source approaches dropout; a subsequent dropout switches the part into 2× mode. Additional features include brightness control by pulse-width modulation of the EN2 pin, prevention of inrush current and excessive input noise during start-up and mode switching, and open/short LED protection. The LTC-3217 costs $1.70 (1000).

Linear Technology Corp, www.linear.com

Phototriac families come in a variety of trigger currents

Reducing EMI-noise harmonics and featuring low peak-operating currents, the VO4157 and VO4158 series of zero-crossing GaAs (gallium-arsenide) infrared LEDs are optically coupled to a photosensitive zero-crossing triac detector chip. Devices in the non-zero-crossing

productroundup

OPTOELECTRONICS/DISPLAYS

VO4257 and VO4258 series of phototriacs can trigger during the ac phase cycle and turn off at the next zero crossing. Both families have 1.6-mA trigger currents, providing a direct interface with microcontrollers and digital circuits; devices with 2- and 3-mA trigger currents are also available. All versions also feature 700 and 800V blocking voltages and isolation for low-voltage logic for 120, 240, and 380V ac lines to control resistive, inductive, or capacitive loads. Available in DIP-6 packages, the devices cost $1.50 (10,000), depending on blocking voltage and input-trigger-current values.

Vishay Intertechnology, www.vishay.com

Series of LED indicators has a variety of options

Available in red, green, yellow, blue, and white, the Q-Series of LED indicators features optional bicolor, tricolor, and flashing LEDs. Additional features include solder-lug/quick-connect terminals, wire terminations, and 200-mm elongated wires. Packaged in 6-, 8-, and 14-mm sizes, the series also comes in prominent-, recessed-, and flush-bezel styles, with bright-chrome, black-chrome, and satin-gray bezel finishes. An integral resistor provides direct connection to 12V dc, 12V ac/dc, 24V dc, 24V ac/dc, 110V ac, and 220V ac. Targeting industrial panels, panel indicators, automation equipment, and industrial-instrumentation applications, the indicators have a viewing angle of 70 to 100°, depending on the model; a 100,000-hour life expectancy; and a −40 to +85°C operating-temperature range.

APEM Components, www.apem.com

Surface-mount LED has 13-cd intensity

This 3.2×1.8×1.75-mm, high-brightness, diffused surface-mount LED features a 13-cd intensity, suiting flash applications. The AOT3218 (advanced-optoelectronic-technology) LED's small package outline includes a 1208 viewing angle with uniform radiation. With a copper-lead-frame construction, the device complies with JEDEC moisture-sensitivity Level 2 requirements. The devices come in blue, red, yellow, green, and RGB surface-mount LEDs.

MRC Components, www.mrccomponents.de

COMPUTERS AND PERIPHERALS

Fast LCD monitors have 4-msec response time

The 17-in. SyncMaster 740BF and 19-in. SyncMaster 940BF LCD monitors feature technologies including MagicSpeed, MagicTune, MagicZone, MagicColor, and MagicBright II. MagicSpeed provides the 4-msec gray-to-gray response time; MagicTune enables control over display features with extensive color-adjustment capability; MagicZone allows the user to select any area of the screen and change its characteristics; MagicColor automatically selects areas in need of color correction and selectively enhances the area; and MagicBright II allows manual selection for setting brightness, contrast, and gamma correction for the currently displayed media type. Analog and digital inputs provide a 700-to-1 contrast ratio, 300 cd/m^2 brightness, 1280×1024 resolution, and 160° viewing angle. The SyncMaster 740BF and SyncMaster 940BF cost $399 and $499, respectively.

Samsung Electronics Co Ltd, www.samsung.com

3-D monitors retain full resolution

Using stereoscopic 3-D technology, the SD1710 StereoMirror display features two 17-in. active-matrix LCD monitors in an up/down configuration, separated at a 110° angle. A semitransparent mirror at a bisecting angle between the two monitors combines with polarizing glasses to gen-

COMPUTERS AND PERIPHERALS

erate the stereo separation. This beam-splitter method creates a stereoscopic 3-D monitor, retaining full resolution, response time, and color saturation from each monitor. The SD1710 costs $3995. **Planar Systems, www.planar.com/stereomirror**

Network hard drive has built-in network-media server

Operating on a Freescale PowerQuicc II MPC8241 processor, the StorCenter network hard drive features a built-in network-media server and Gigabit Ethernet speed. Features include 160- and 250-Gbyte capacities, IAB (Iomega Automatic Backup) Pro software, a 7200-rpm drive, and UPnP compliance. Two USB 2.0 ports provide expansion capabilities as well as support for external USB hubs, permitting four additional USB 2.0 storage devices and two USB 2.0 printers to attach simultaneously to each drive. The 160-Gbyte StorCenter costs $199.99, a 250-Gbyte version with 8-Mbyte cache costs $289.99, and a 1-Tbyte model will be available early in 2006. **Iomega Corp, www.iomega.com**

Hard-drive kit converts notebook hard drives into external hard drives

Converting a notebook hard drive into an external hard drive, the Travelstar upgrade kit comprises a 2.5-in. hard drive in 40-, 60-, 80-, and 100-Gbyte capacities; installation instructions; the Apricorn EZ Gig II hard-drive-cloning and upgrade software; and a USB 2.0 hard-drive enclosure. The USB 1.1-compatible kit includes a 1m USB cable and auxiliary power cables. Prices for the stand-alone hard drives range from $109 to $189; prices for upgrade kits range from $139 to $219. **Hitachi Global Storage Technologies, www.hitachigst.com**

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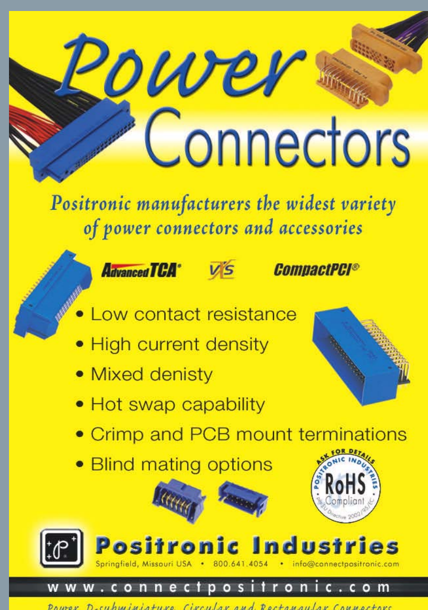
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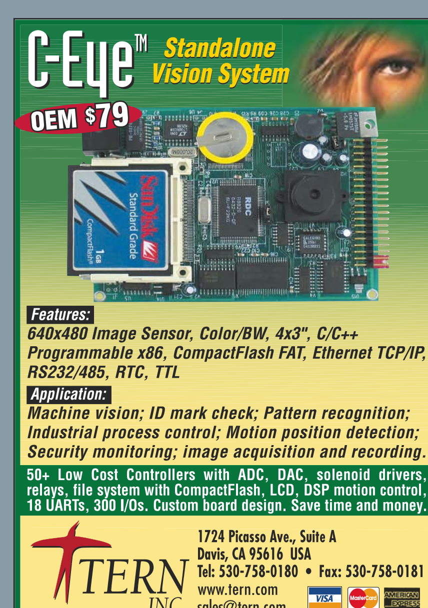
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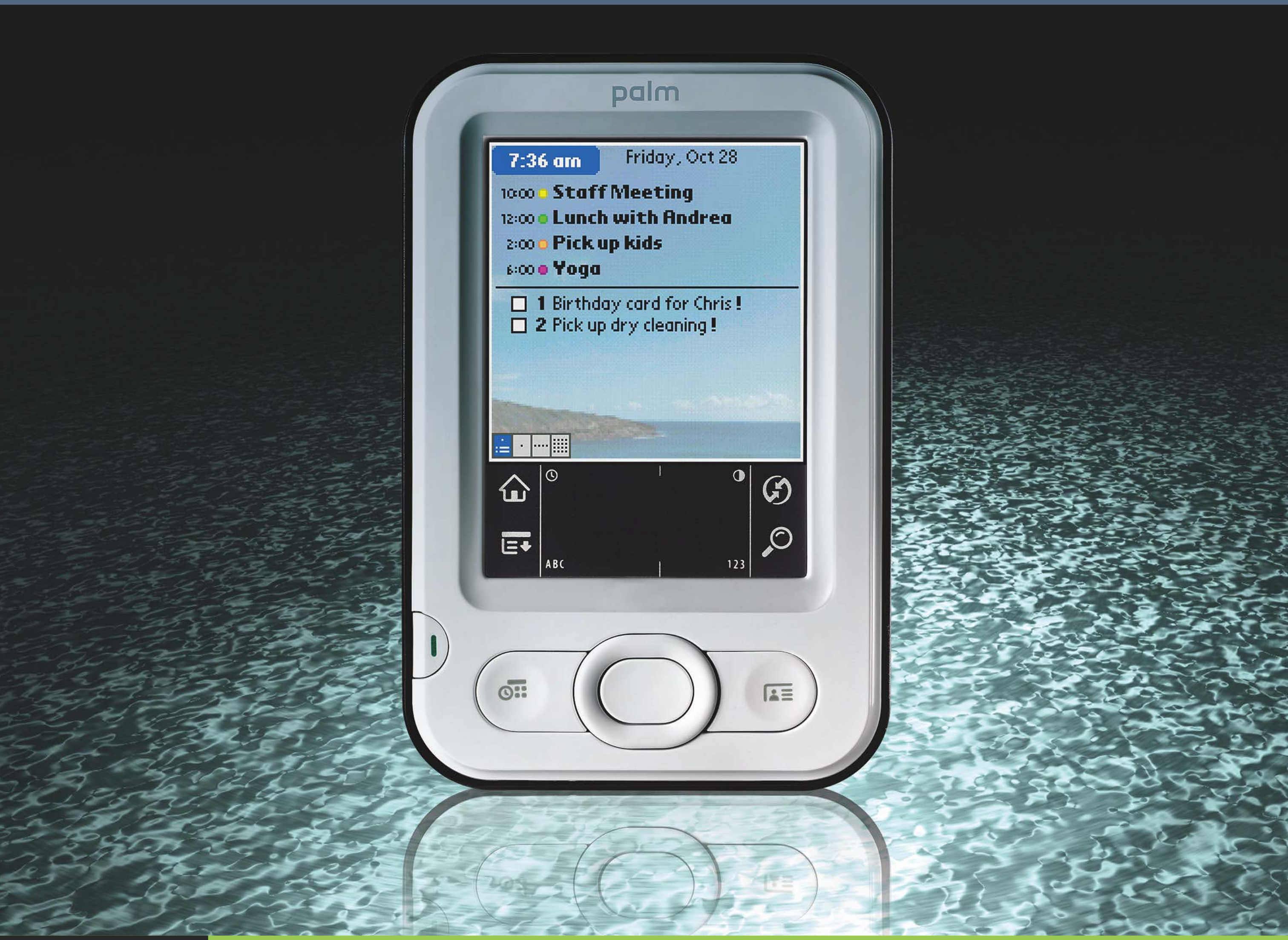

STATS Entry-level price: $99 / 2004 sales: 1.97 million units

PDAs yield to smart phones and media players

Few products that have enjoyed the volume-market success of the PDA have had such a short run when it comes to popularity. Palm Pilots went from being a novelty in 1997 to megahit status around the turn of the century. But the stand-alone PDA may just disappear before its 10th birthday. According to market-research company NPD Group, retail sales reached 3.68 million units in 2001 but dropped to fewer than 2 million in 2004. That plummet comes at a time when PDAs are more value-packed than ever. In 2000 and 2001, leading-edge units cost more than $500. Today, the entry-level $99 Palm Zire packs far more features, and even the $350 Tungsten that integrates wireless and multimedia support is a relative bargain.

Around 2000, it appeared that the PDA would usurp the mobile-phone function. Instead, tiny smart phones today include most of the functions that PDAs offer. Only a niche group of business-e-mail users insists on a BlackBerry or a Palm Treo phone in the PDA form factor. Many businesspeople and, certainly, consumers carry a music player and a phone but no PDA. Indeed, consumers increasingly use iPods and other hard-disk-equipped digital-media players to store and transport contacts, calendars, and even office data files, along with music, photos, and video.

—by Maury Wright

Flawed reality

Our Oct 27, 2005, Reality Check incorrectly stated that the original design of the Denver airport's ill-fated luggage-handling system used Invensys Systems' Wonderware InTouch. *EDN* regrets the error. Go to www.edn.com/article/CA6275425 for details.

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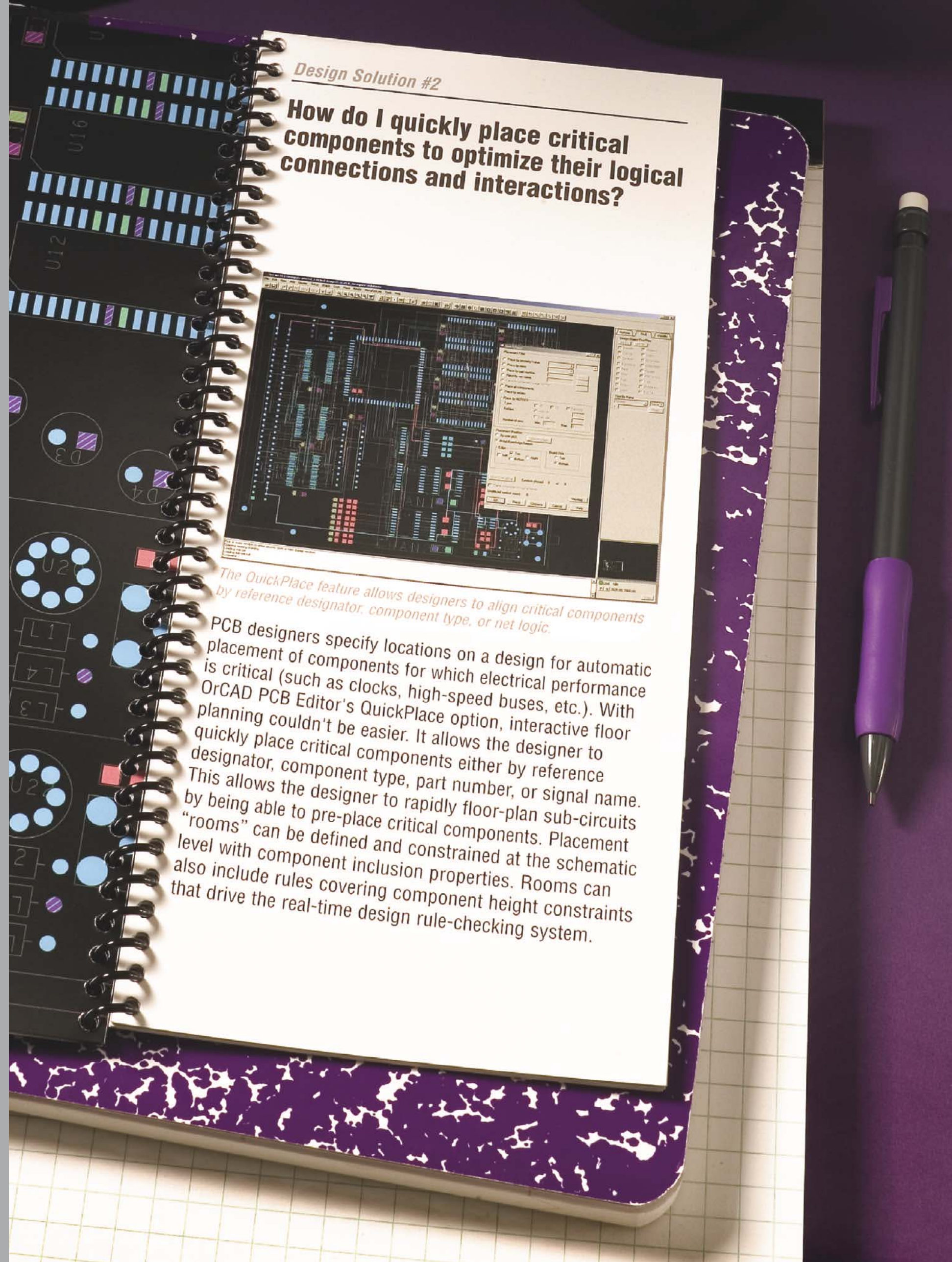

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